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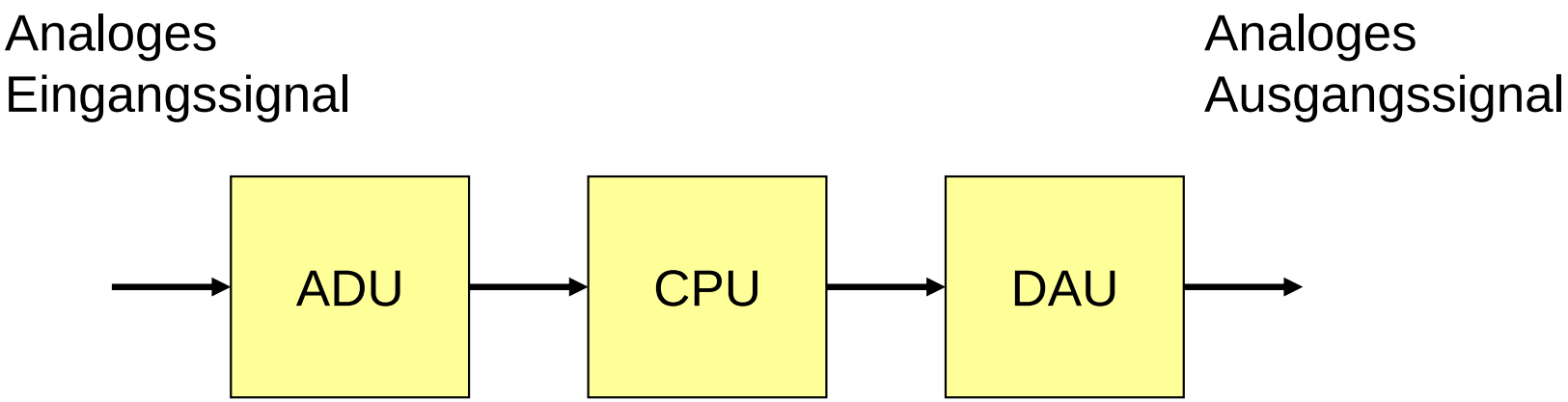
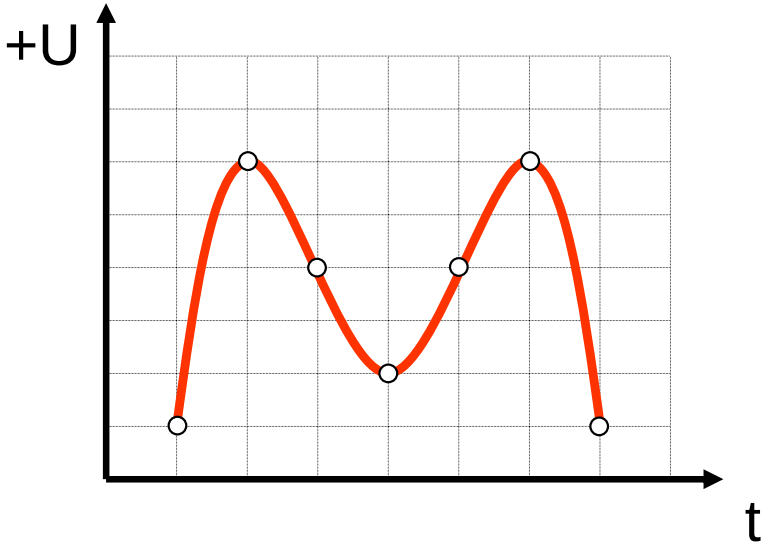
# Kapitel 7:
# AD- und DA-Umsetzer

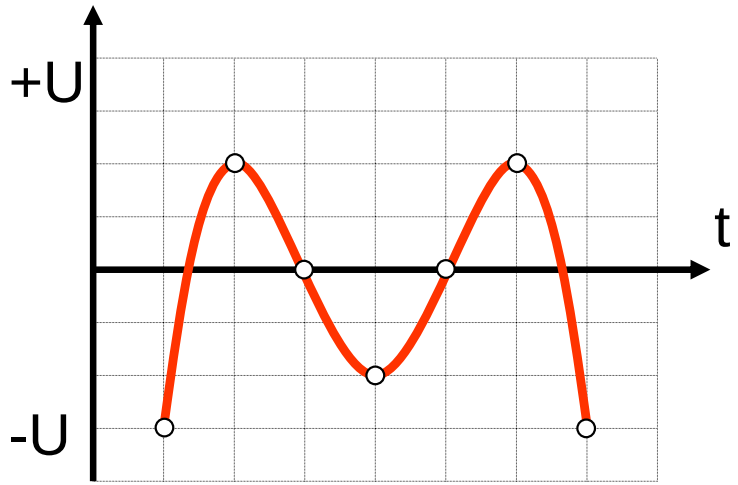
- Analoge Signale und Codierungen
- DA-Umsetzer
  - DA-Umsetzer mit gewichteten Widerständen
  - DA-Umsetzer mit R2R Netzwerk
- AD-Umsetzer
  - Inkrementalumsetzer
  - Sägezahnumsetzer
  - Track&Hold Schaltung
  - Sample&Hold Schaltung
  - Sukzessive Approximation
  - Parallelumsetzer
  - Dual-Slop-Umsetzer
- Wandlerfenster
- Anwendungsbeispiele


Analoges
Eingangssignal
Analoges
Ausgangssignal
ADU
CPU
DAU

# Signale und Formate
## Unipolare Ein-/Ausgangssignale



# Signale und Formate
## Bipolare Ein-/Ausgangssignale



# Signale und Formate

## Standartsignale zur Analogkopplung

Analogsignale

- Spannungssignale
  - unipolar
    - 0...1V
    - 0..5V
    - 0..15V
    - 0..10V
    - 0..24V
    - 0..60V
  - bipolar
    - -1...+1V
    - -2,5...+2,5V
    - -5...+5V
    - -10...+10V
    - -15...+15V
- Stromsignale
  - unipolar
    - 0...20mA
    - 4..20mA
    - 0..1A
  - bipolar
    - -20...+20mA
    - -1...+1A
    - -5...+5A

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| Unipolar Bitmuster | | |
|---|---|---|
| 11111111 | 255 | 5V |
| 11111110 | 254 | |
| 11111101 | 253 | |
| ..... | | |
| 00000001 | 1 | |
| 00000000 | 0 | 0V |

$$\Delta U_A = \frac{U_{A\max}}{2^n - 1}$$

$$\Delta U_A = \frac{5V}{2^8 - 1} = 0{,}0196078\,V$$

# Signale und Formate

## Vorzeichen Betragscodierung Sign Magnitude Coding

| | |
|---|---|
| 0 1111 1111 255 | 1 1111 1111 255 |
| ..... | ..... |
| 0 0000 0001 1 | 1 0000 0001 1 |
| 0 0000 0000 0 | 1 0000 0000 0 |
| 1 0000 0001 -1 | 0 0000 0001 -1 |
| ..... | ..... |
| 1 1111 1110 -254 | 0 1111 1110 -254 |
| 1 1111 1111 -255 | 0 1111 1111 -255 |

1 1111 1111  255
.....
1 0000 0001  1
1 0000 0000  0
0 1111 1111 -1
.....
0 0000 0001 -254
0 0000 0000 -255

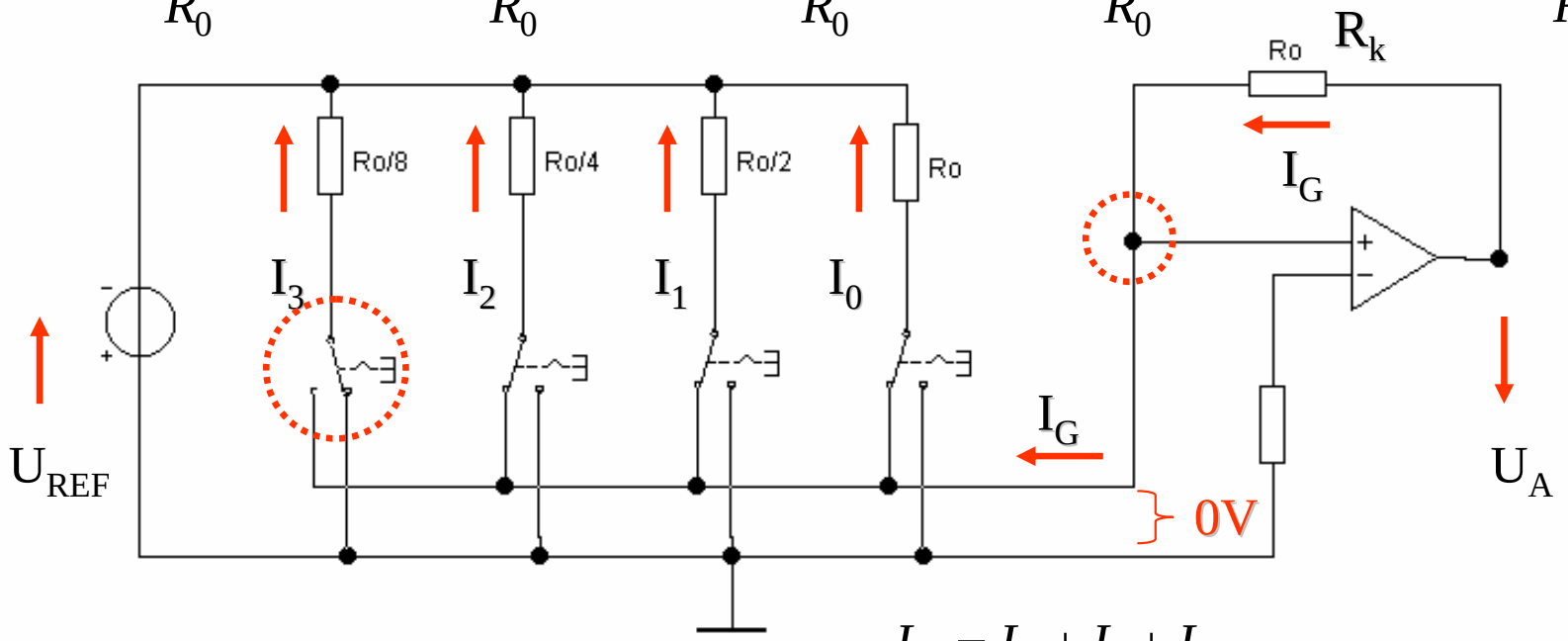
0 1111 1111 +255
.....
0 0000 0001 +1
0 0000 0000 0
1 1111 1111 -1
.....
1 0000 0001 -255
1 0000 0000 -256

# DA-Umsetzer
## Verfahren

- Gewichtete Widerstandsnetzwerke
- R-2R-Netzwerken
- 1Bit PWM-Umsetzer

# DA-Umsetzer
## mit gewichteten Widerständen

$$I_3 = 8 \cdot \frac{U_{REF}}{R_0} \quad I_2 = 4 \cdot \frac{U_{REF}}{R_0} \quad I_1 = 2 \cdot \frac{U_{REF}}{R_0} \quad I_0 = 1 \cdot \frac{U_{REF}}{R_0} \qquad I_G = \frac{U_A}{R_k}$$




$$I_G = I_2 + I_1 + I_0$$

# DA-Umsetzer
## mit gewichteten Widerständen

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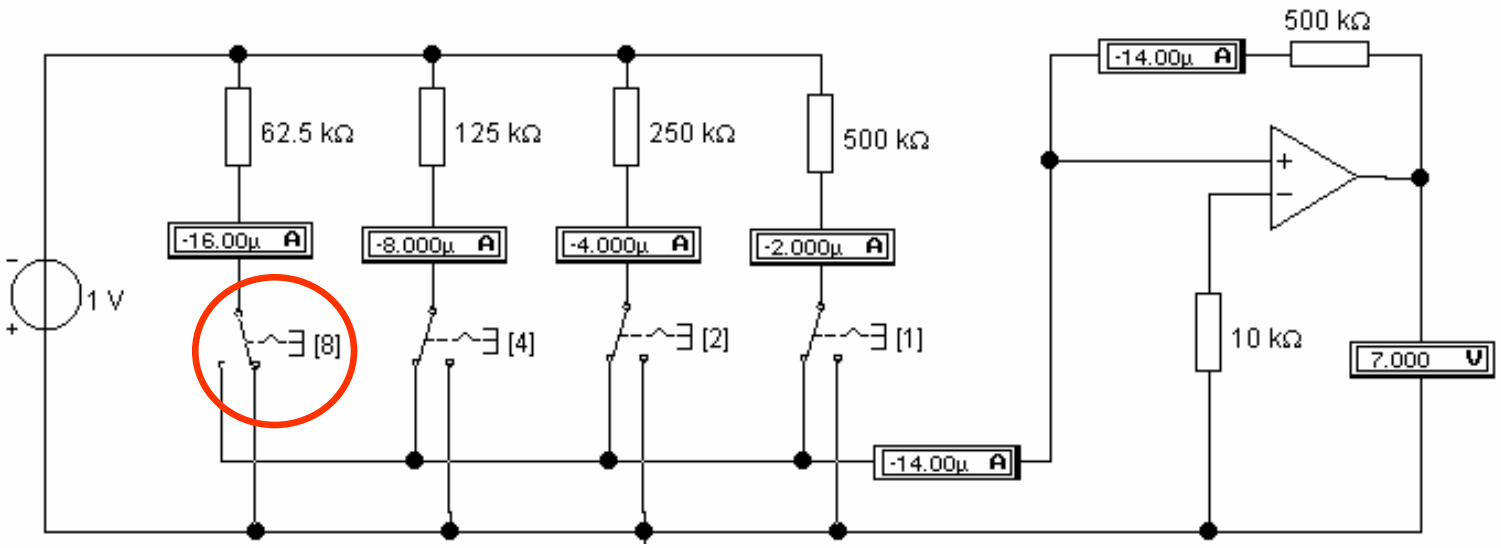
$$U_A = \left(I_3 \cdot S_3 + I_2 \cdot S_2 + I_1 \cdot S_1 + I_0 \cdot S_0\right) \cdot R_k$$

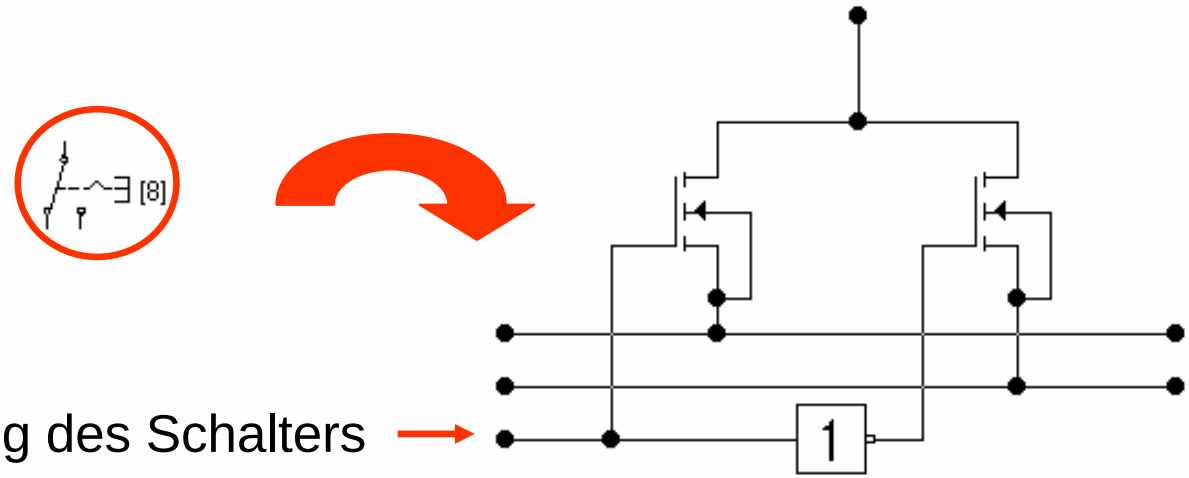
$$U_{Rk} = U_A = -\left(8 \cdot \frac{-U_{REF}}{R_0} \cdot S_3 + 4 \cdot \frac{-U_{REF}}{R_0} \cdot S_2 + 2 \cdot \frac{-U_{REF}}{R_0} \cdot S_1 + 1 \cdot \frac{-U_{REF}}{R_0} \cdot S_0\right) \cdot R_k$$

$$U_{Rk} = U_A = \left(2^{n-1} \cdot S_{n-1} + 2^{n-2} \cdot S_{n-2} + \ldots + 2^0 \cdot S_0\right) \cdot U_{REF} \cdot \frac{R_k}{R_0}$$

$$U_{A\max} = \left(2^n - 1\right) \cdot U_{REF} \cdot \frac{R_k}{R_0}$$

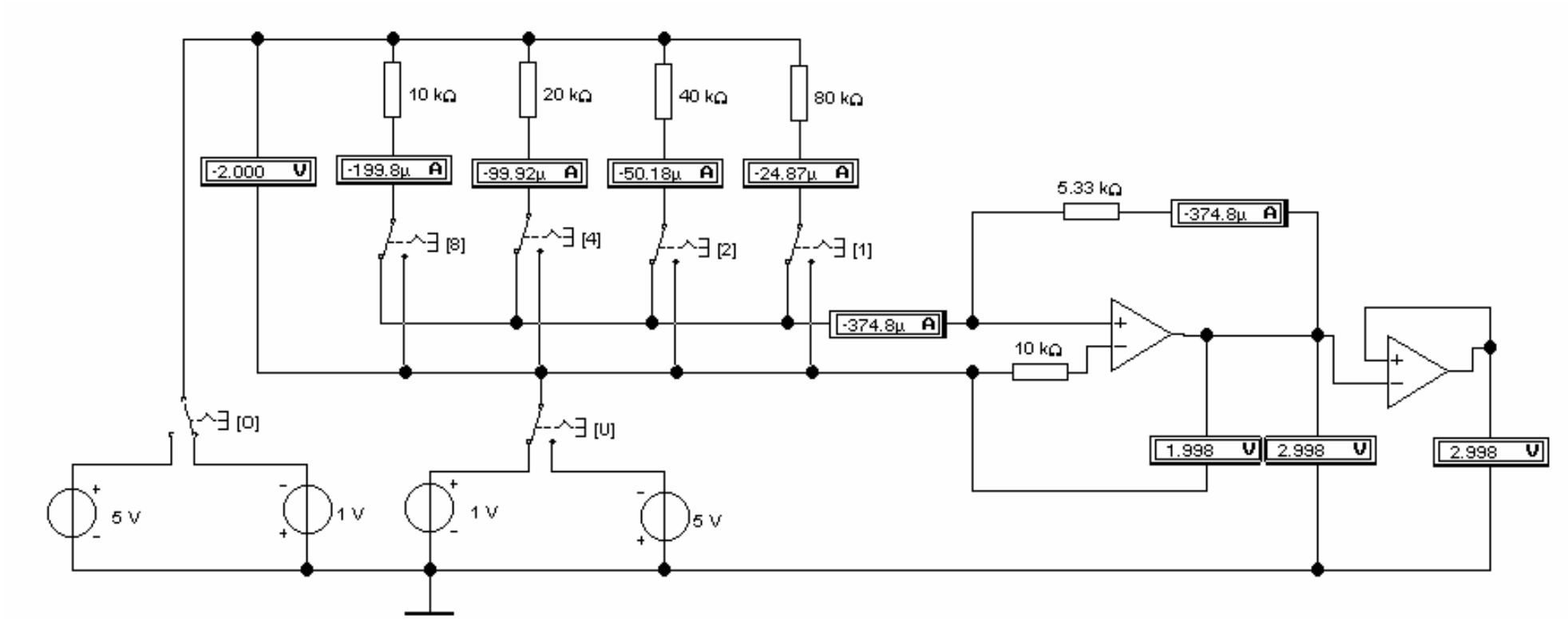
# DA-Umsetzer
## mit gewichteten Widerständen



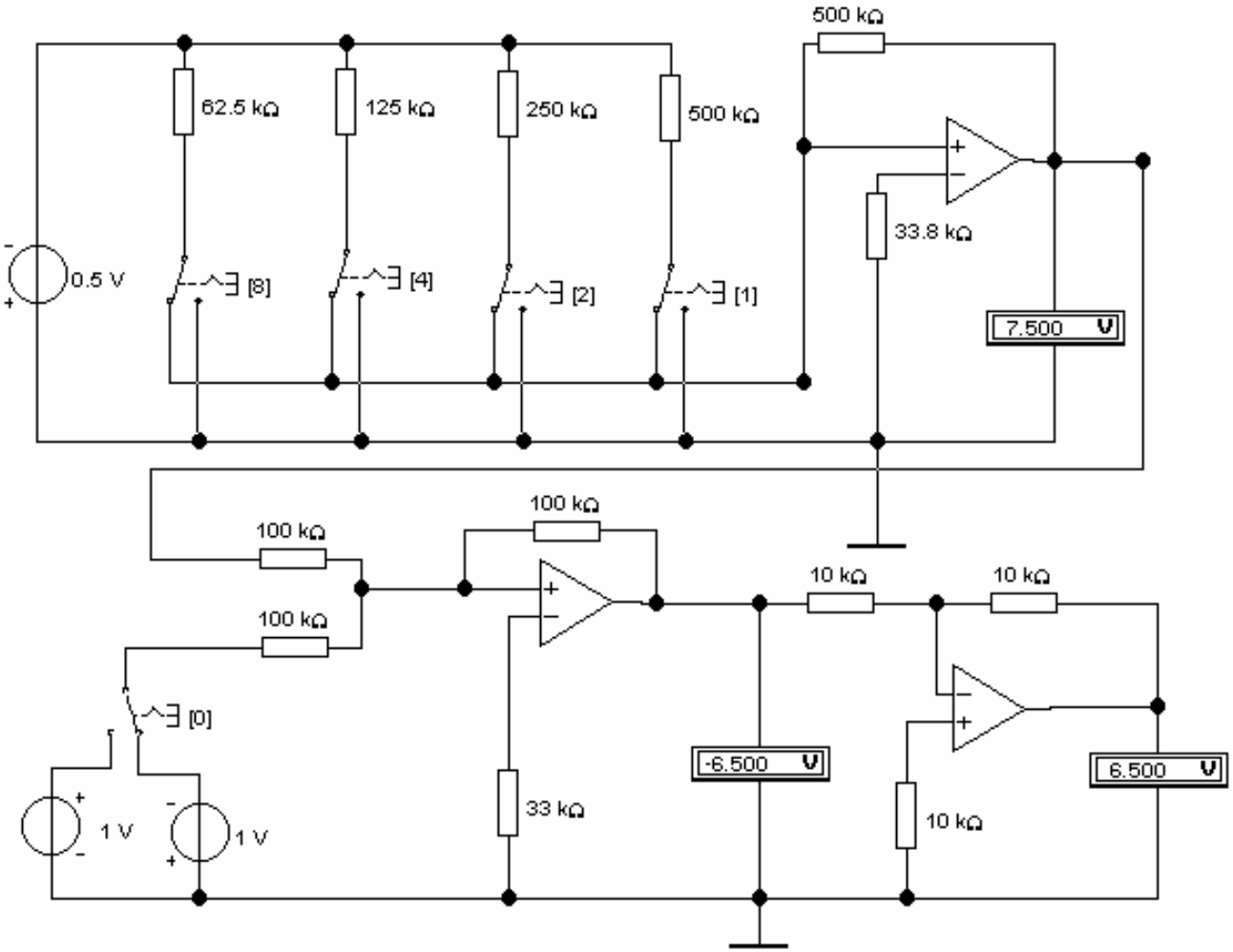




Ansteuerung des Schalters →

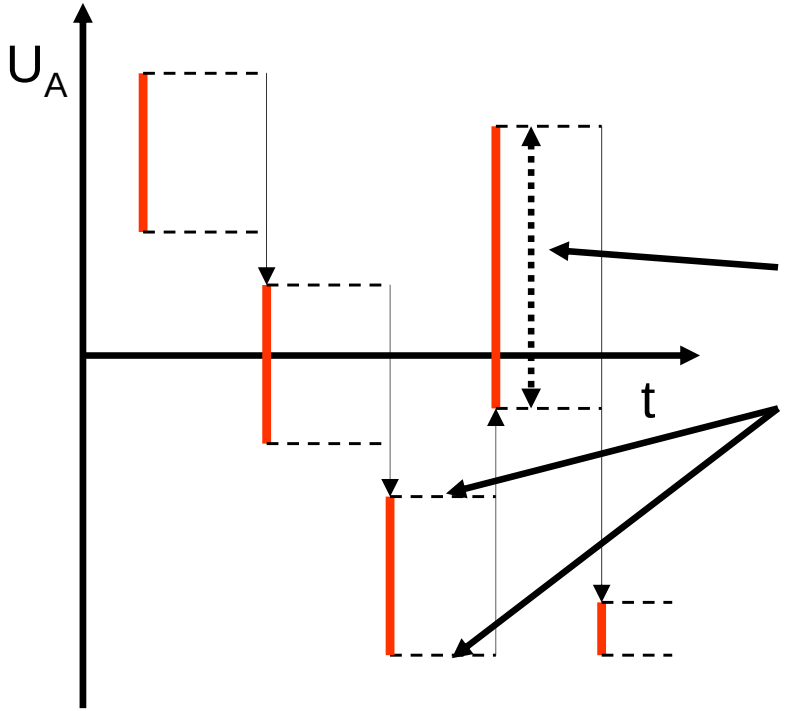
# DA-Umsetzer
## bipolar mit wählbarem Ausgangsbereich



# DA-Umsetzer
## bipolar mit wählbarem Ausgangsbereich



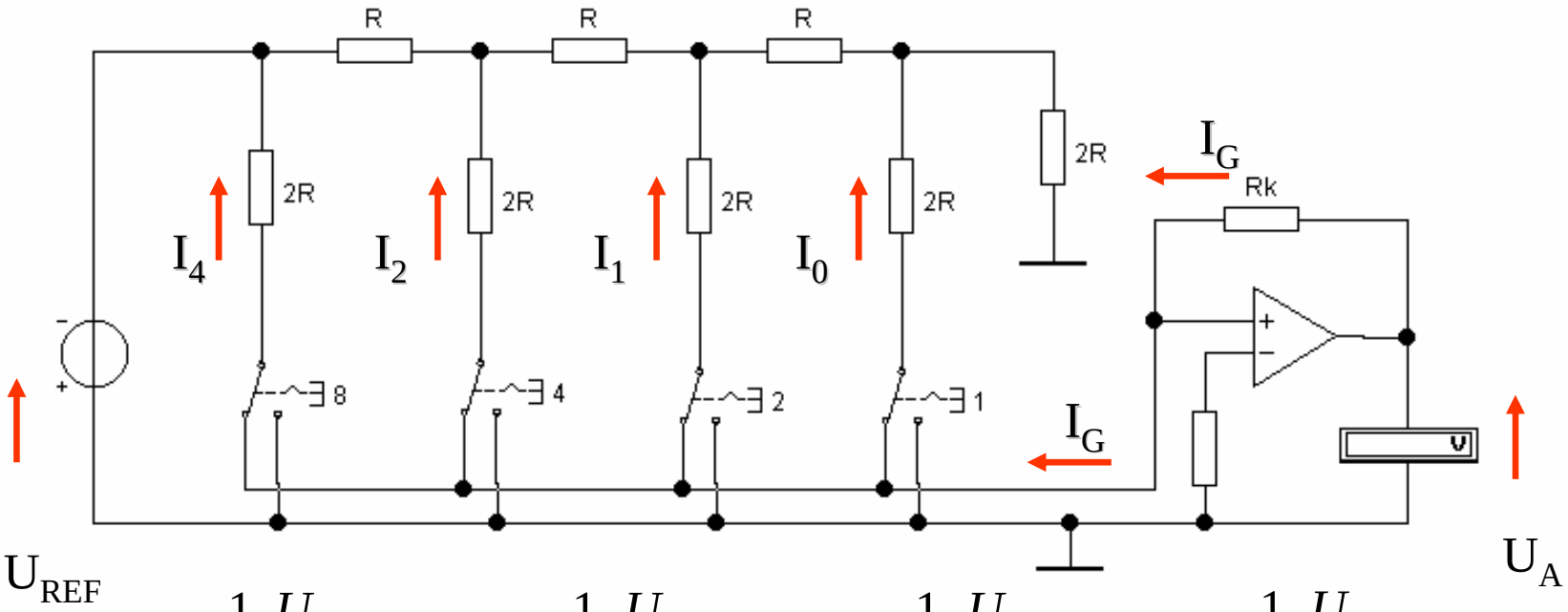
# DA-Umsetzer
## $U_A$ wählbar




In jedem Fenster die gleiche Bitbreite.

Der untere und obere Wert für $U_A$ ist über einstellbare Referenzspannungen wählbar.

# DA-Umsetzer
## mit R-2R-Netzwerk




$$I_3 = \frac{1}{1} \cdot \frac{U_{REF}}{2R} \qquad I_2 = \frac{1}{2} \cdot \frac{U_{REF}}{2R} \qquad I_1 = \frac{1}{4} \cdot \frac{U_{REF}}{2R} \qquad I_0 = \frac{1}{8} \cdot \frac{U_{REF}}{2R}$$

# DA-Umsetzer
## mit R-2R-Netzwerk

$$U_{Rk} = U_A = \left(I_3 \cdot S_3 + I_2 \cdot S_2 + I_1 \cdot S_1 + I_0 \cdot S_0\right) \cdot R_k$$

$$U_{Rk} = U_A = -\left(\frac{1}{1} \cdot \frac{-U_{REF}}{2R} \cdot S_3 + \frac{1}{2} \cdot \frac{-U_{REF}}{2R} \cdot S_2 + \frac{1}{4} \cdot \frac{-U_{REF}}{2R} \cdot S_1 + \frac{1}{8} \cdot \frac{-U_{REF}}{2R} \cdot S_0\right) \cdot R_k$$

$$U_{Rk} = U_A = \left(8 \cdot S_3 + 4 \cdot S_2 + 2 \cdot S_1 + 1 \cdot S_0\right) \cdot \frac{U_{REF} \cdot R_k}{8 \cdot 2R}$$

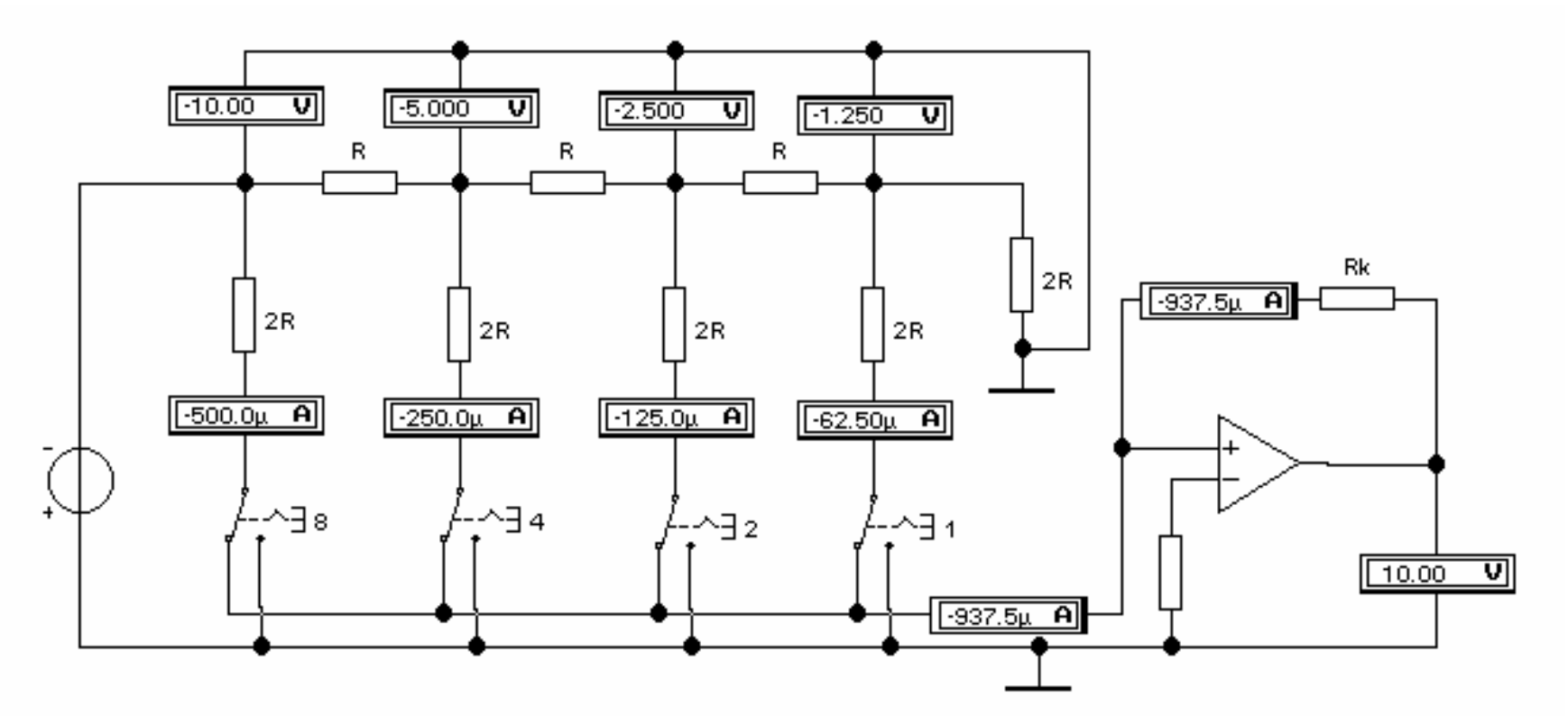
$$U_{Rk} = U_A = \left(2^{n-1} \cdot S_{n-1} + 2^{n-2} \cdot S_{n-2} + \ldots + 2^0 \cdot S_0\right) \cdot \frac{U_{REF} \cdot R_k}{2^{n-1} \cdot 2R}$$

bei $R_k = R$

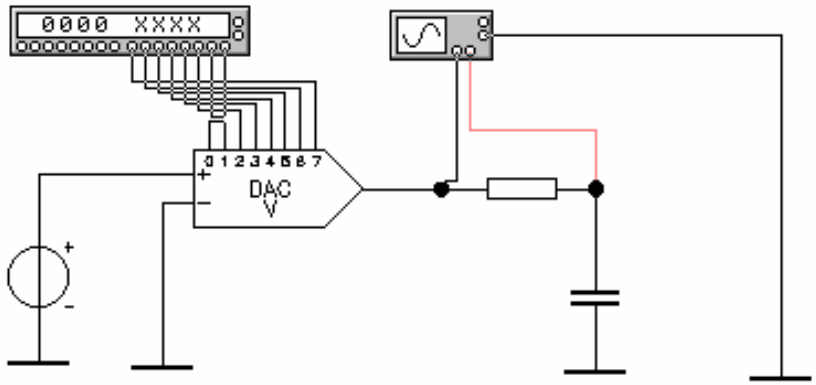
$$U_{Rk} = U_A = \left(2^{n-1} \cdot S_{n-1} + 2^{n-2} \cdot S_{n-2} + \ldots + 2^0 \cdot S_0\right) \cdot \frac{U_{REF}}{2^n}$$

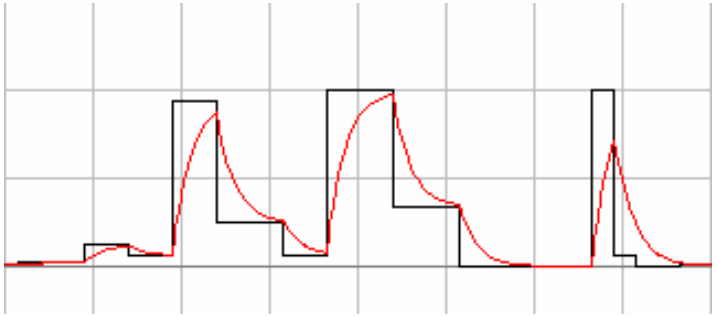
$$U_{A\max} = \left(2^n - 1\right) \cdot \frac{U_{REF}}{2^n}$$

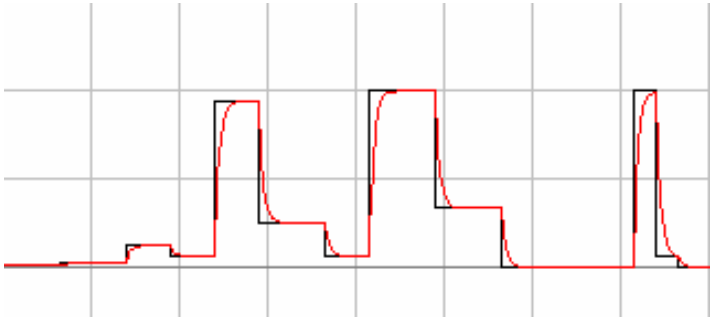
# DA-Umsetzer
## mit R-2R Netzwerk



# DA-Umsetzer
## Analogsignalfilterung



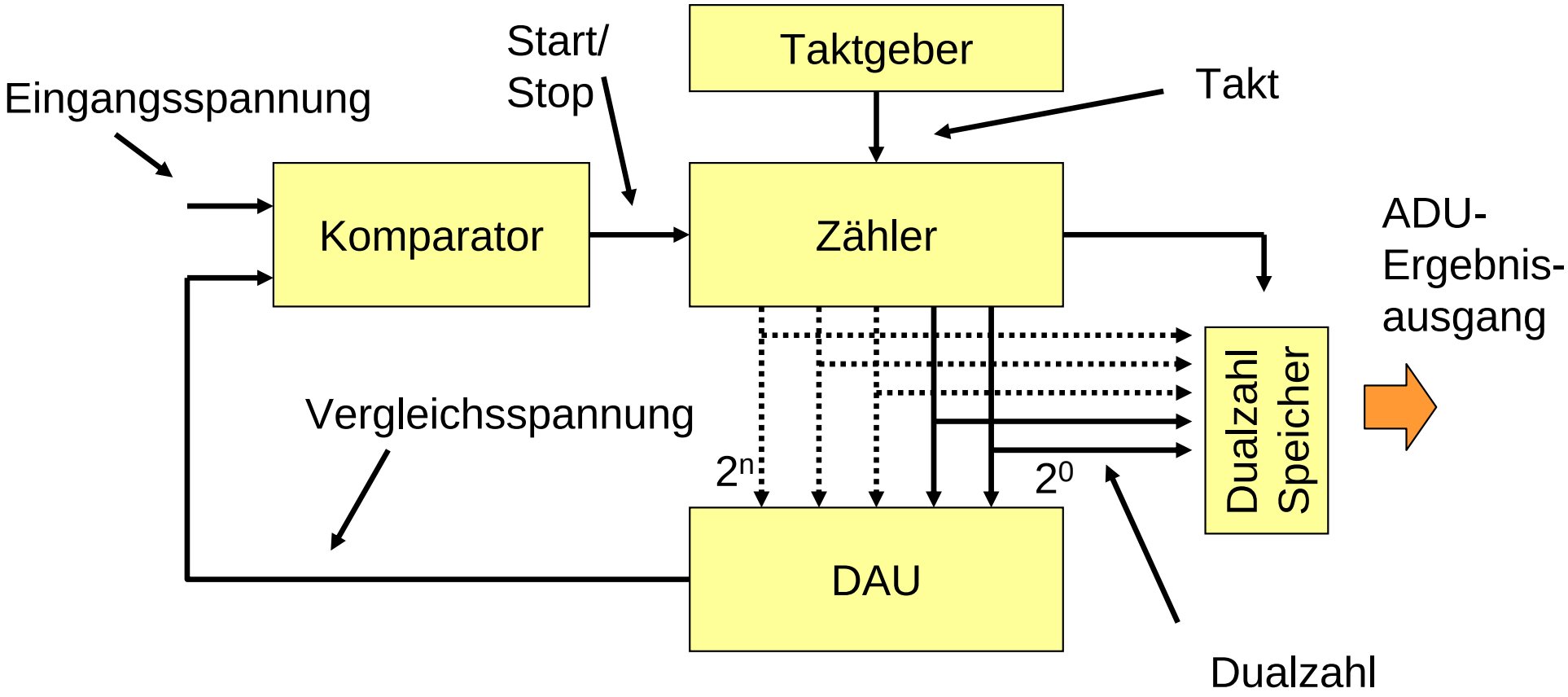


Die gestufte Ausgangsspannung kann mit einem Tiefpassfilter in einen kontinuierlichen Spannungverlauf umgeformt werden.

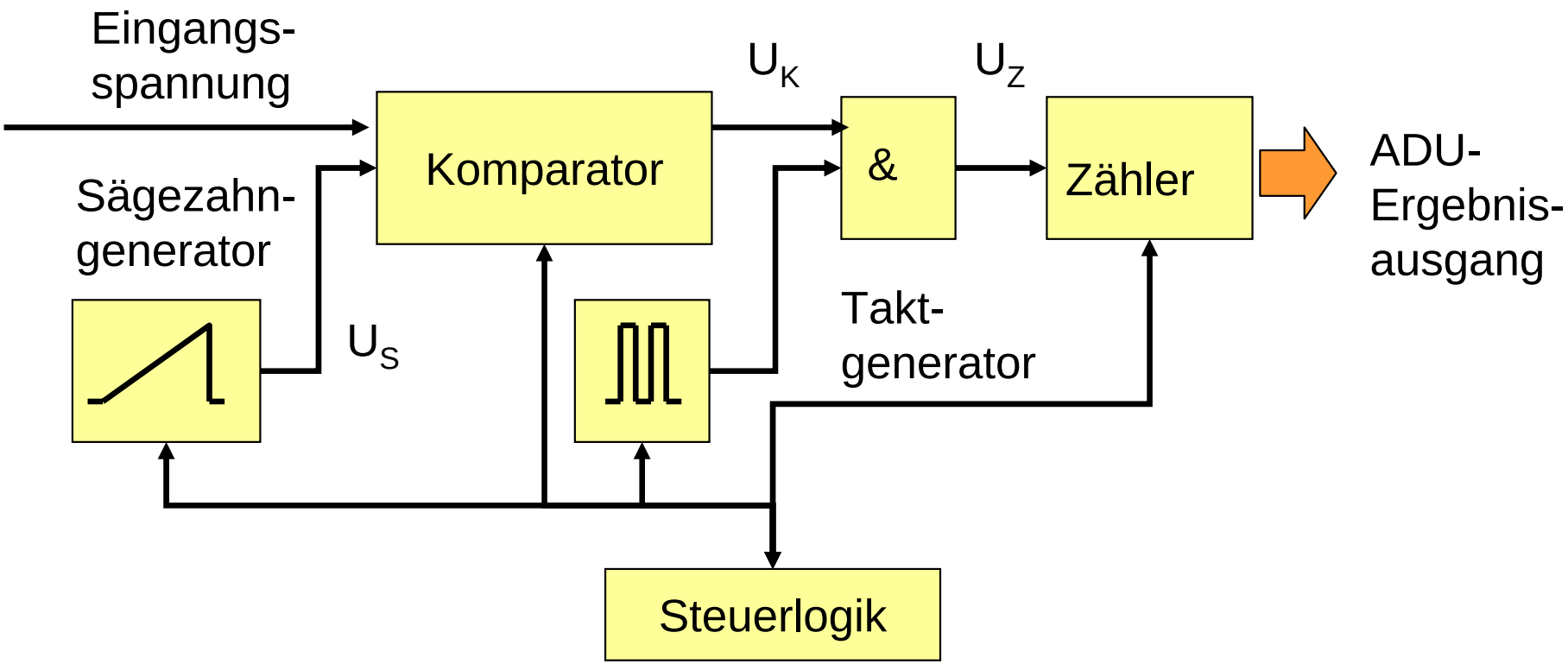
# AD-Umsetzer
## Verfahren

- Inkrementalumsetzer
- Sägezahnumsetzer
- Parallelumsetzer
- Sukzessive Approximation
- Dual-Slope-Umsetzer

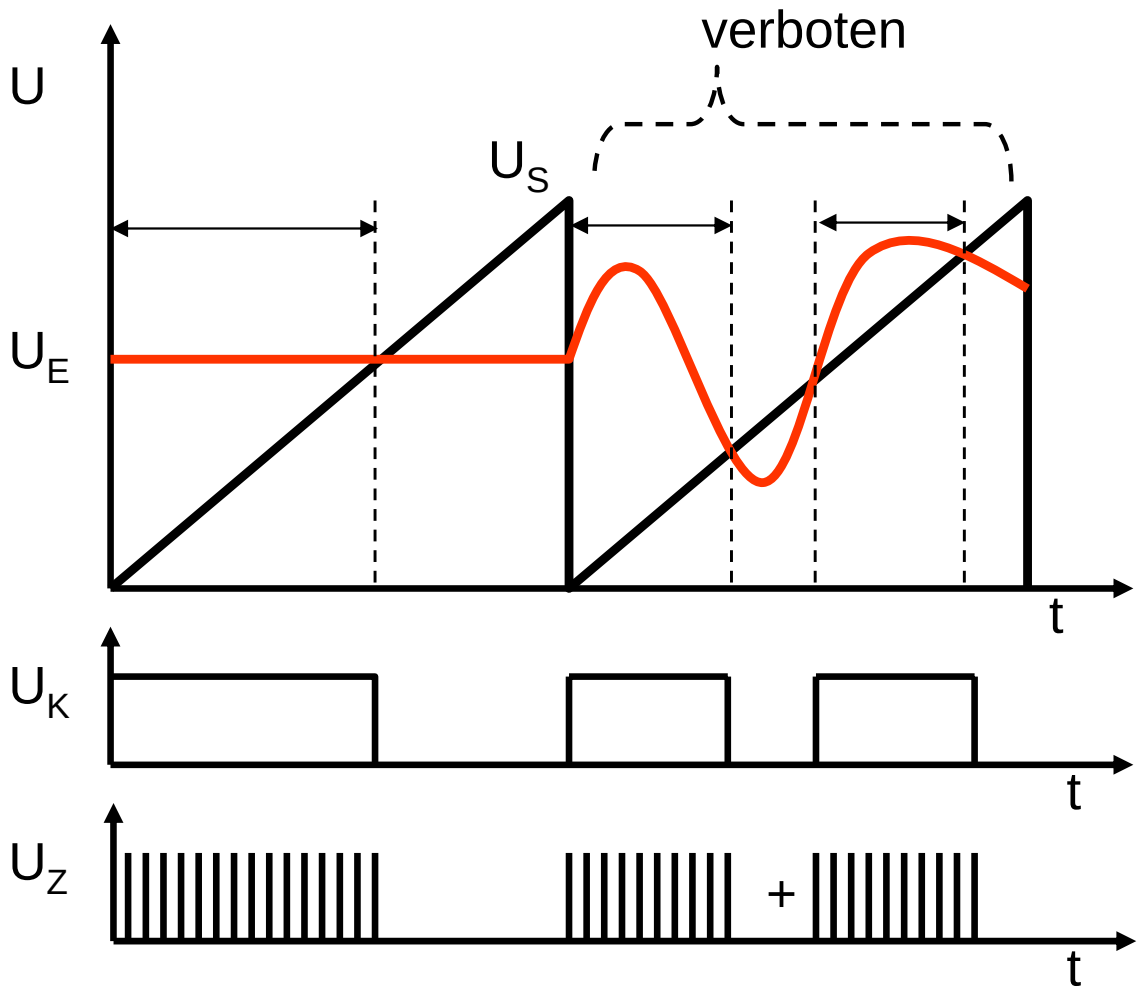
# AD-Umsetzer
## Inkrementalumsetzer



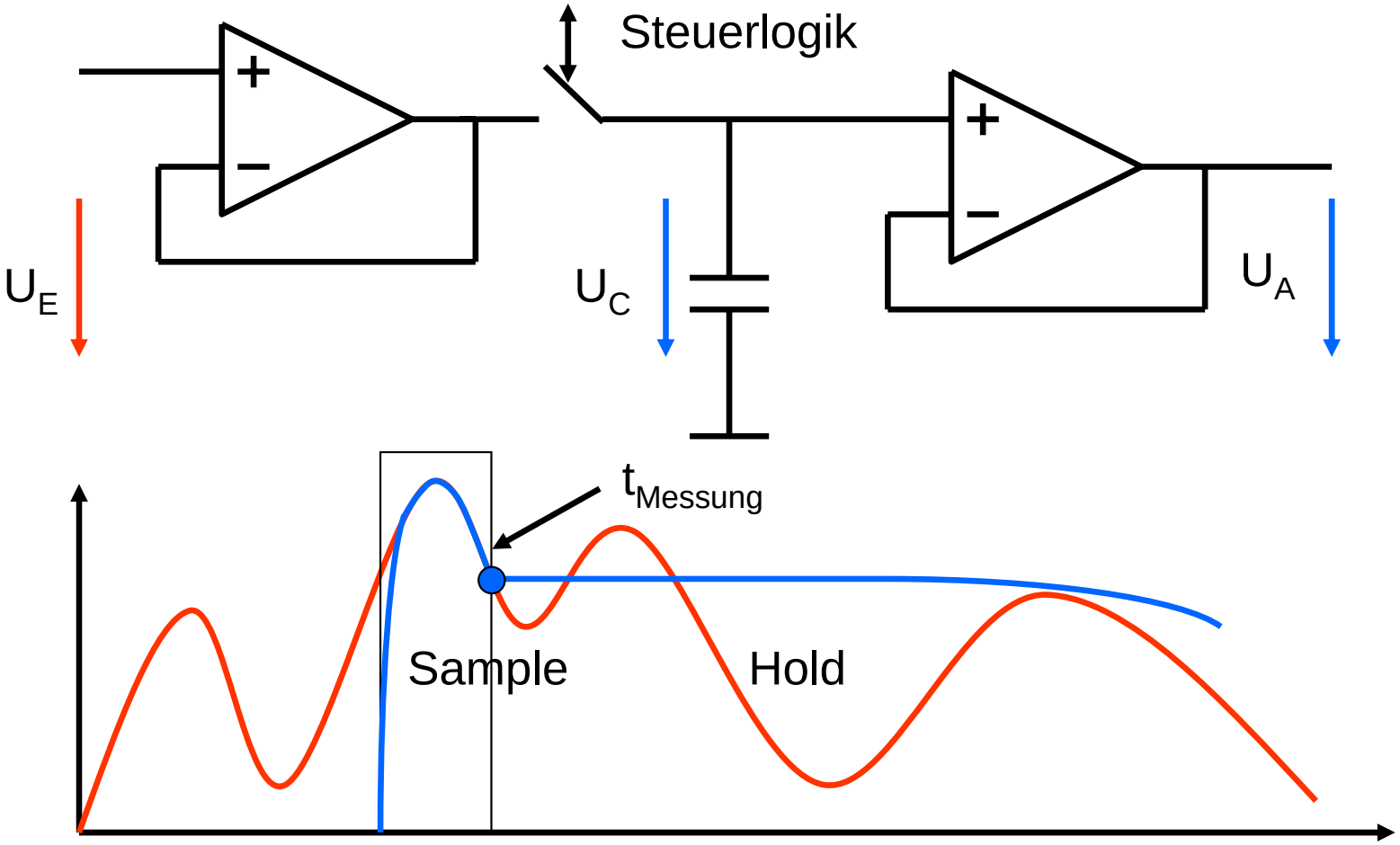
# AD-Umsetzer
## Sägezahnumsetzer



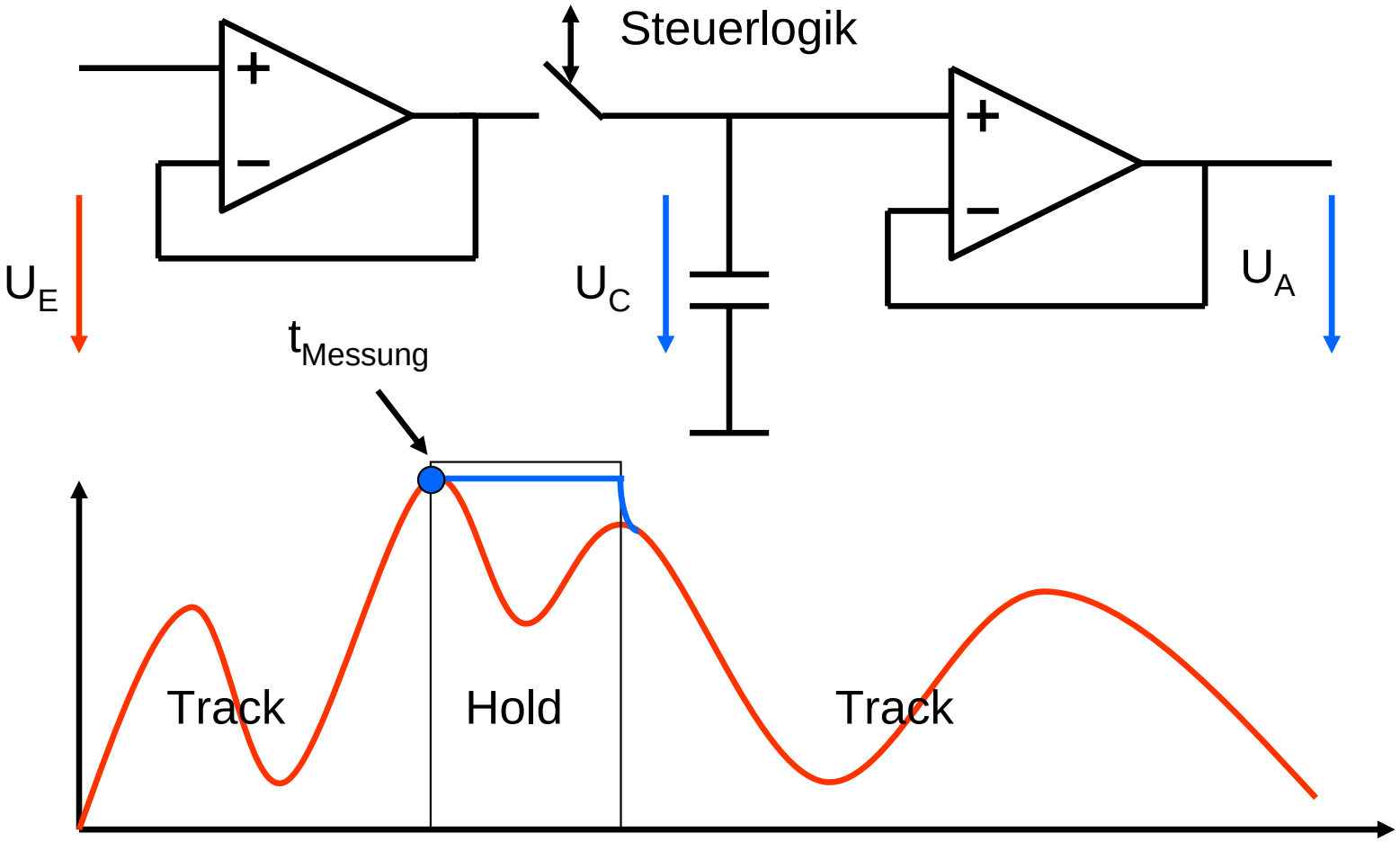
# AD-Umsetzer
## Sägezahnumsetzer



# Sample & Hold Schaltung



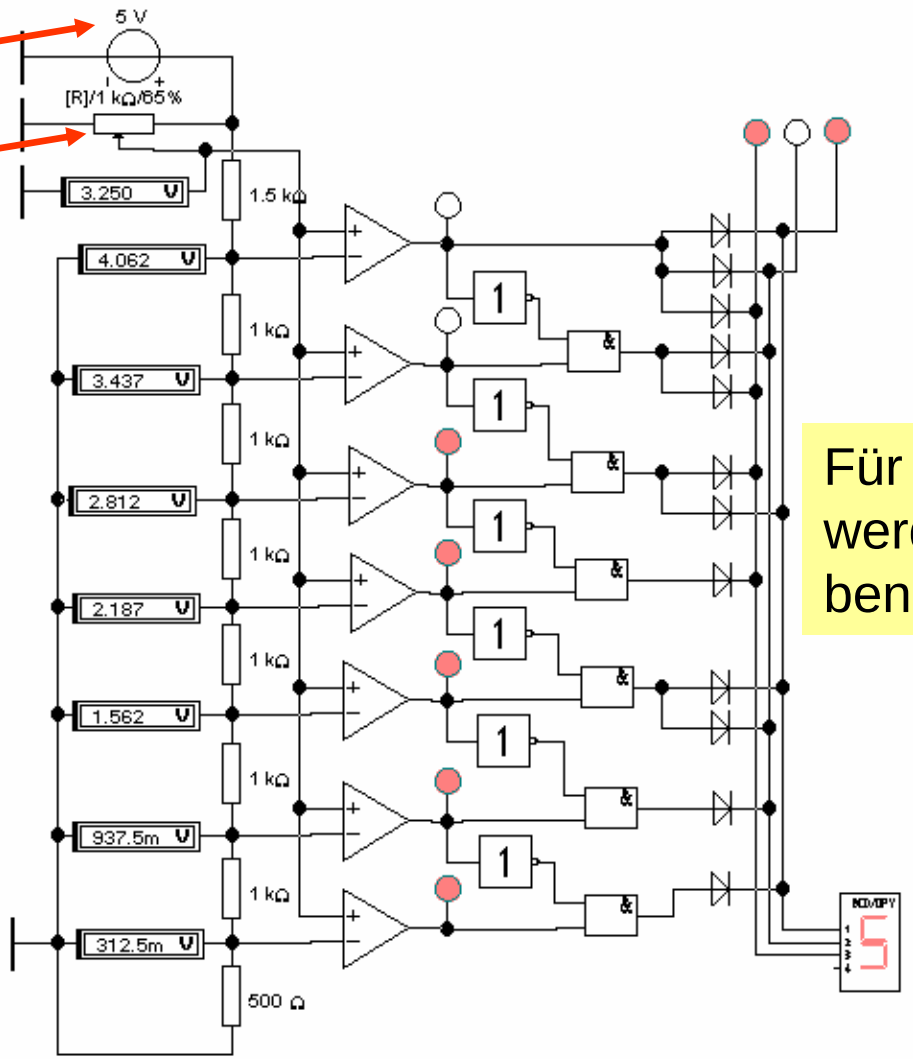
# Track & Hold Schaltung



# AD-Umsetzer
## Parallelumsetzer

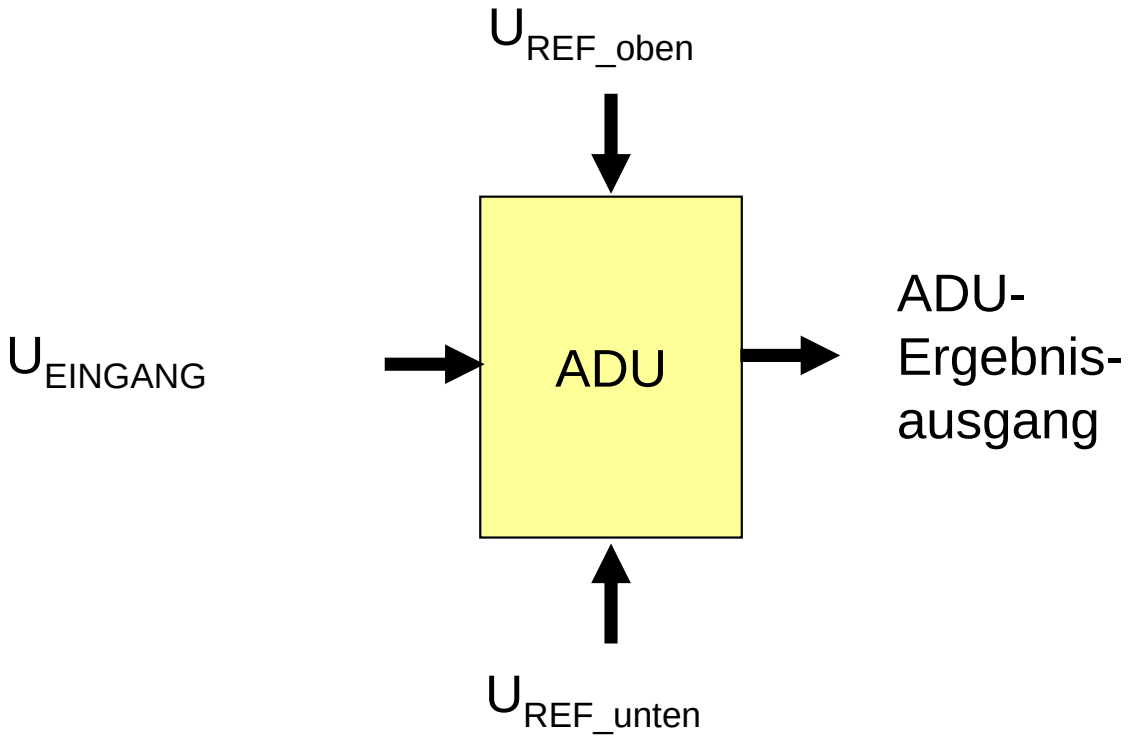
Referenzspannung

Eingangsspannung über ein Potentiometer bereitgestellt.

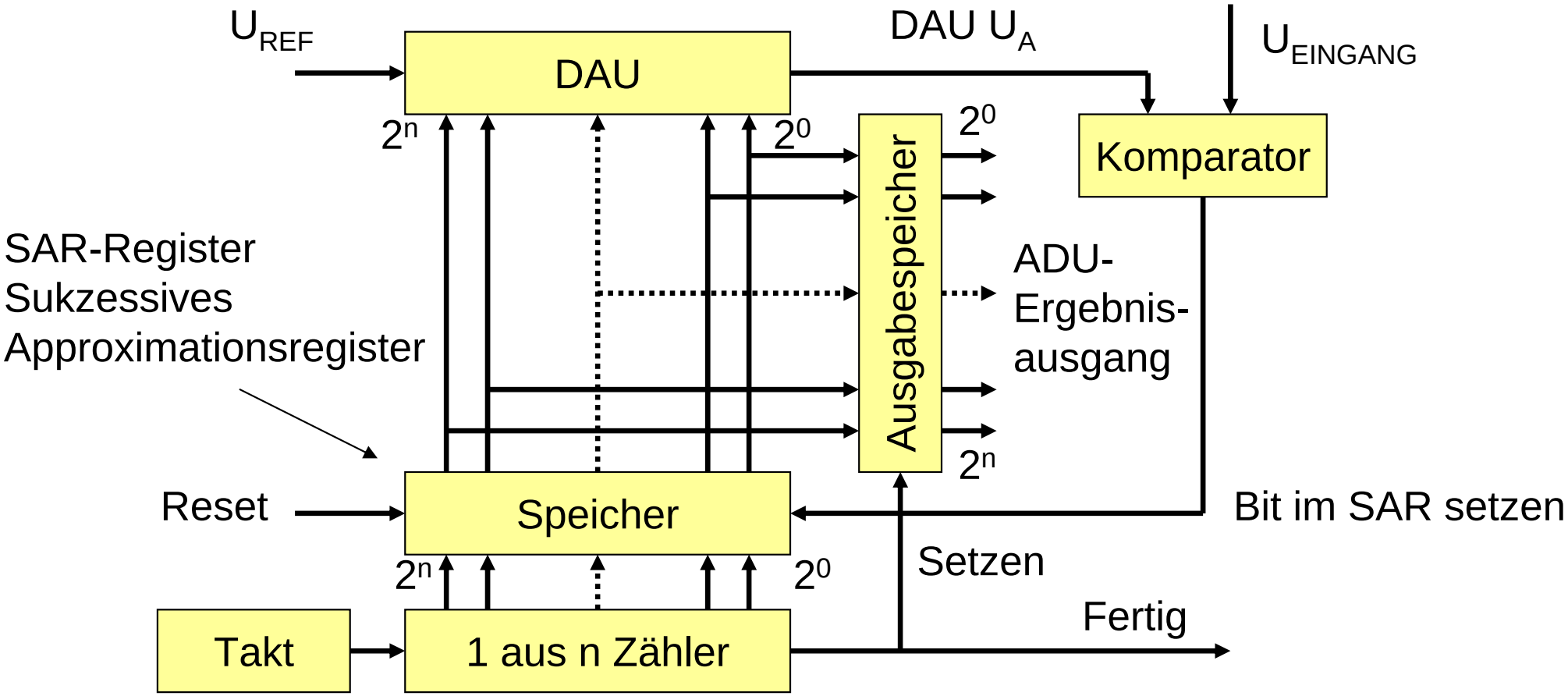



Für 12 Bit Wandlerbreite werden 4096 Komparatoren benötigt

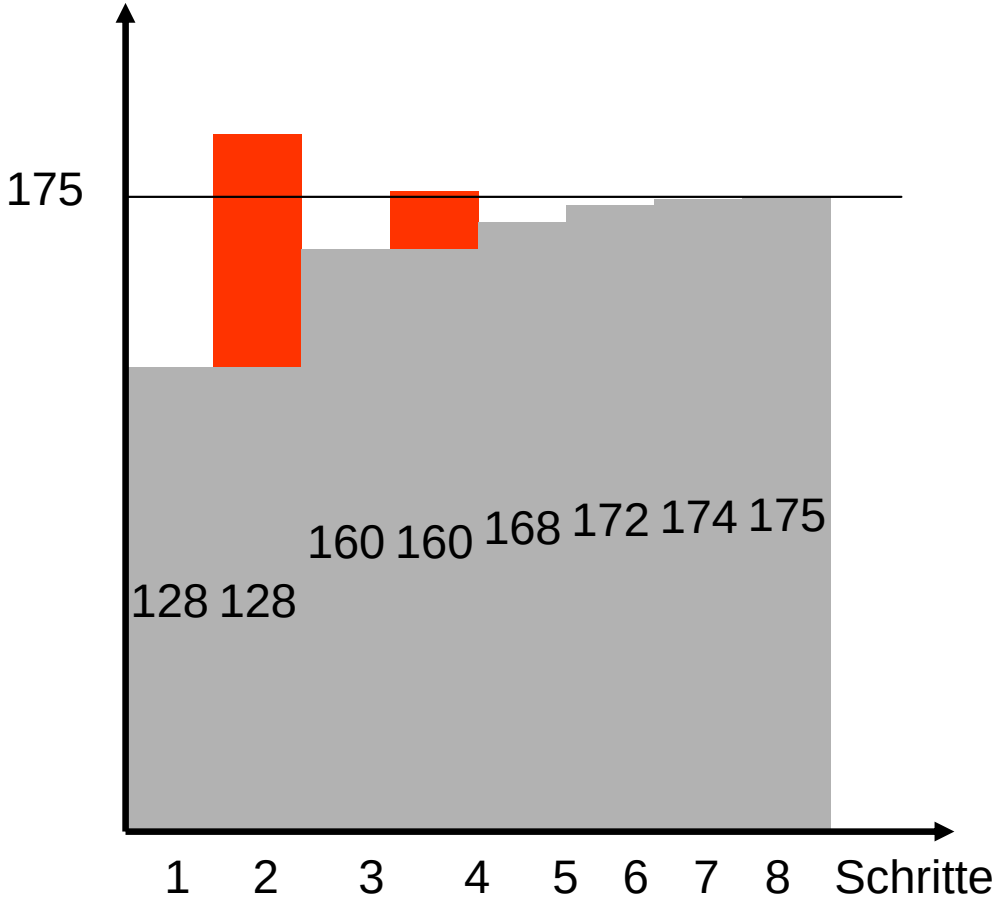
# AD-Umsetzer
## Wandlerfensterfestlegung



# AD-Umsetzer
## Sukzessive Approximation

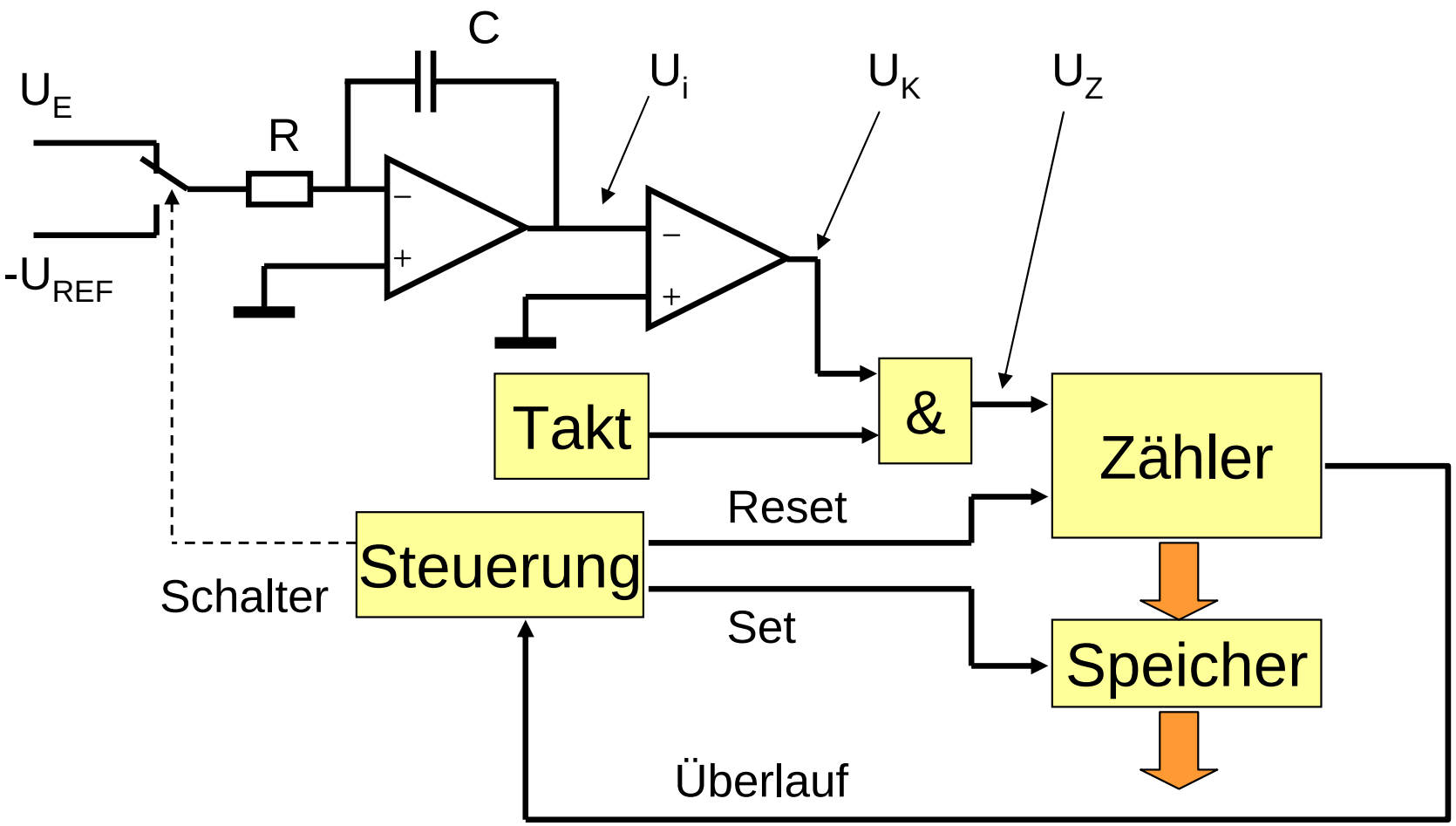


# AD-Umsetzer
## Sukzessive Approximation

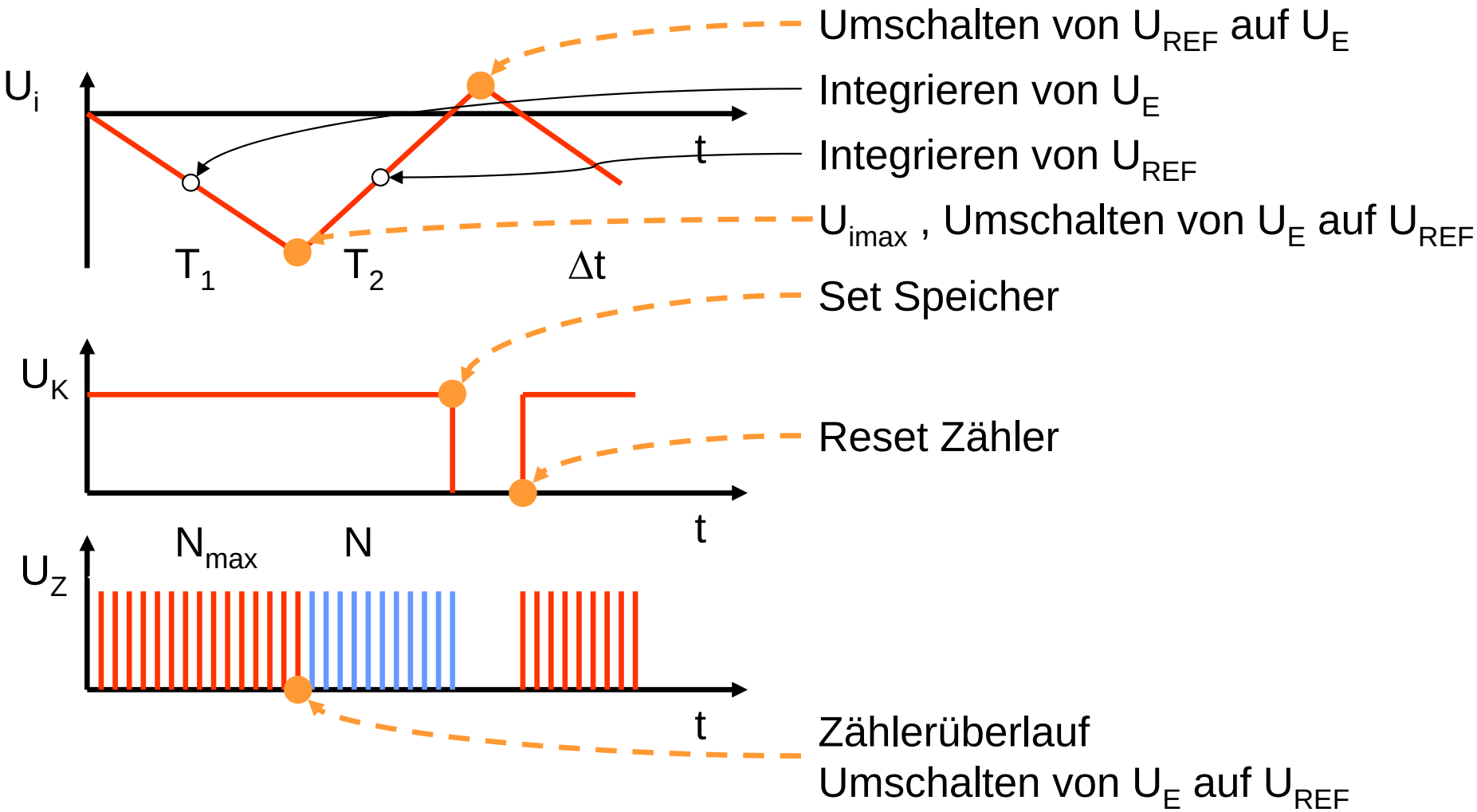



| $2^7$ | $2^6$ | $2^5$ | $2^4$ | $2^3$ | $2^2$ | $2^1$ | $2^0$ |
|---|---|---|---|---|---|---|---|
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0 |
| 1 | 0 | 1 | 0 | 1 | 1 | 0 | 0 |
| 1 | 0 | 1 | 0 | 1 | 1 | 1 | 0 |
| 1 | 0 | 1 | 0 | 1 | 1 | 1 | 1 |

# AD-Umsetzer
## Dual-Slope Verfahren



# AD-Umsetzer
## Dual-Slope Verfahren



$$u_{i\max} = -\frac{1}{\tau_i}\int_0^{T_1} u_E \cdot dt$$

$$u_{i\max} = -\frac{T_1}{\tau_i}\cdot u_E$$

$$\tau_i = R \cdot C$$

$$T_1 = T_0 \cdot N_{\max}$$

$f_0$-Taktgenerator

$$f_0 = \frac{1}{T_0}$$

$$u_{i\max} = -\frac{N_{\max}\cdot T_0}{\tau_i}\cdot u_E$$

Durch Umschalten von $U_E$ auf $U_{REF}$ wird bis zum Zeitpunkt $u_i$=0 integriert.

$$u_i = u_{i\max} + \left(-\frac{1}{\tau_i}\cdot\int U_{REF}\cdot dt\right) = u_{i\max} - \frac{1}{\tau_i}\cdot U_{REF}\cdot t$$

$$u_i = 0 = u_{i\max} - \frac{1}{\tau_i}\cdot U_{REF}\cdot T_2$$

$$T_2 = N \cdot T_0$$

$$0 = u_{i\max} - \frac{1}{\tau_i}\cdot U_{REF}\cdot N\cdot T_0$$

$$0 = u_{i\max} - \frac{1}{\tau_i} \cdot U_{REF} \cdot N \cdot T_0$$

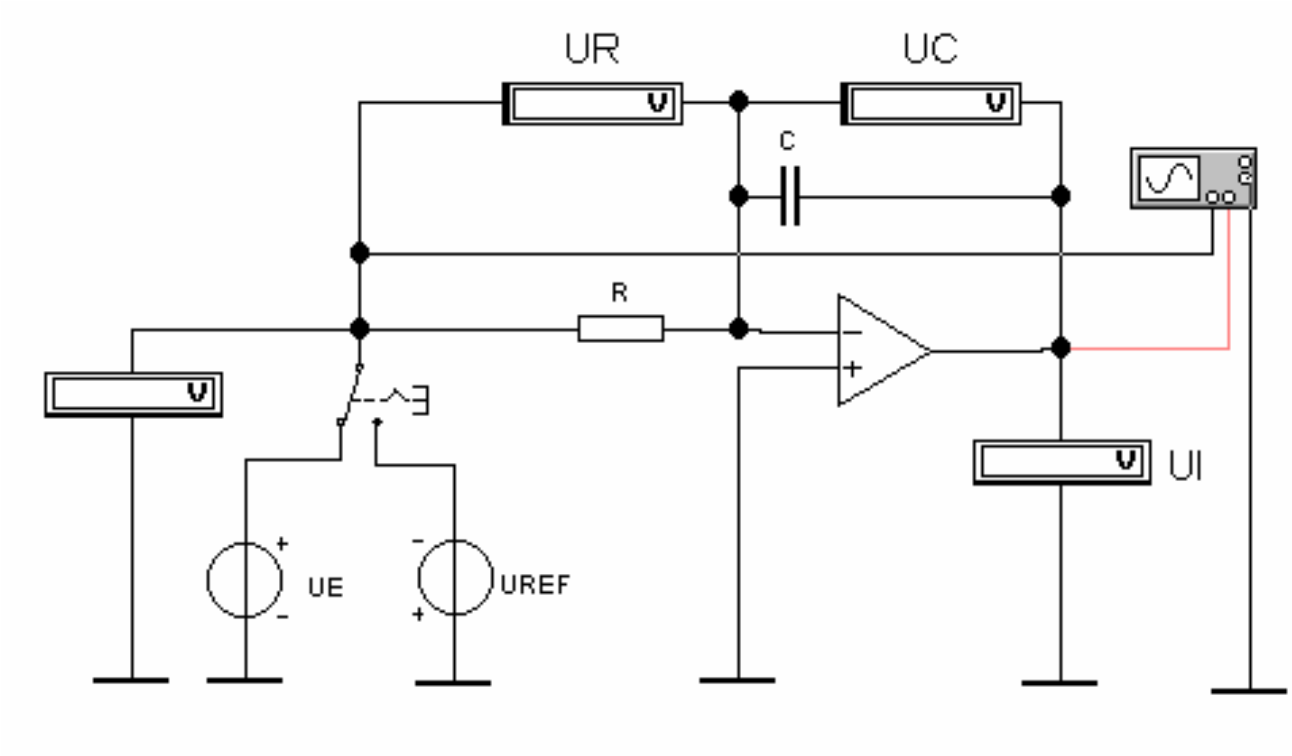
$$u_{i\max} = \frac{1}{\tau_i} \cdot U_{REF} \cdot N \cdot T_0$$

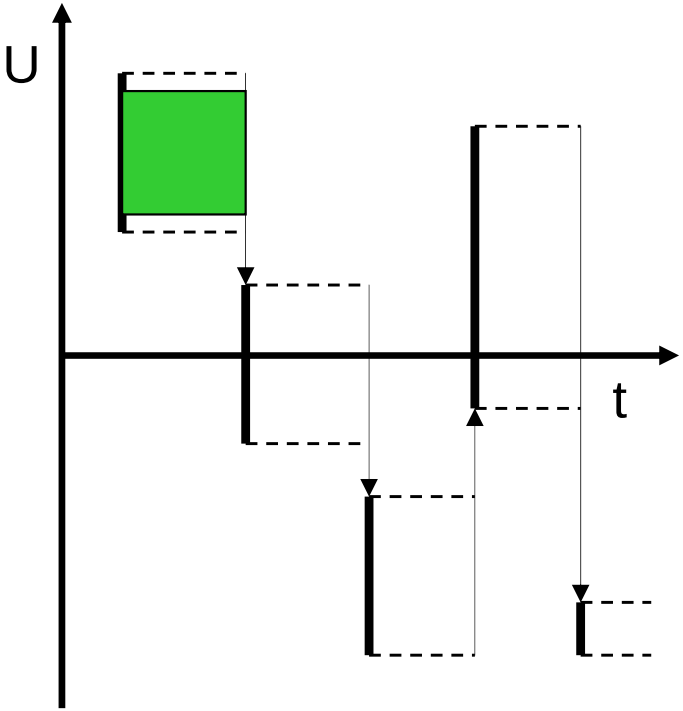
$$\frac{-N_{\max} \cdot T_0}{\tau_i} \cdot u_E = \frac{1}{\tau_i} \cdot U_{REF} \cdot N \cdot T_0$$

$$\boxed{u_{i\max} = -\frac{N \cdot T_0}{\tau_i} \cdot u_E}$$

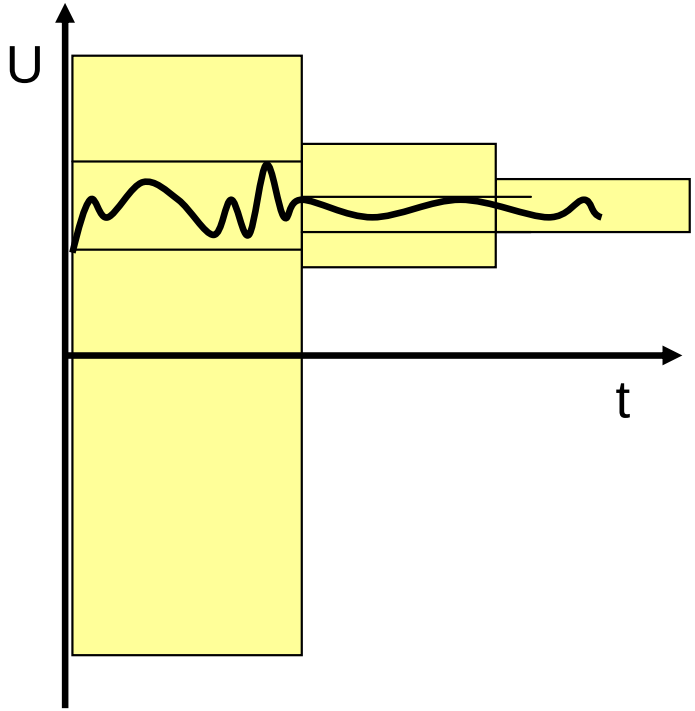
$$\boxed{u_E = -U_{REF} \cdot \frac{N}{N_{\max}}}$$

# AD-Umsetzer
## Dual-Slope Verfahren



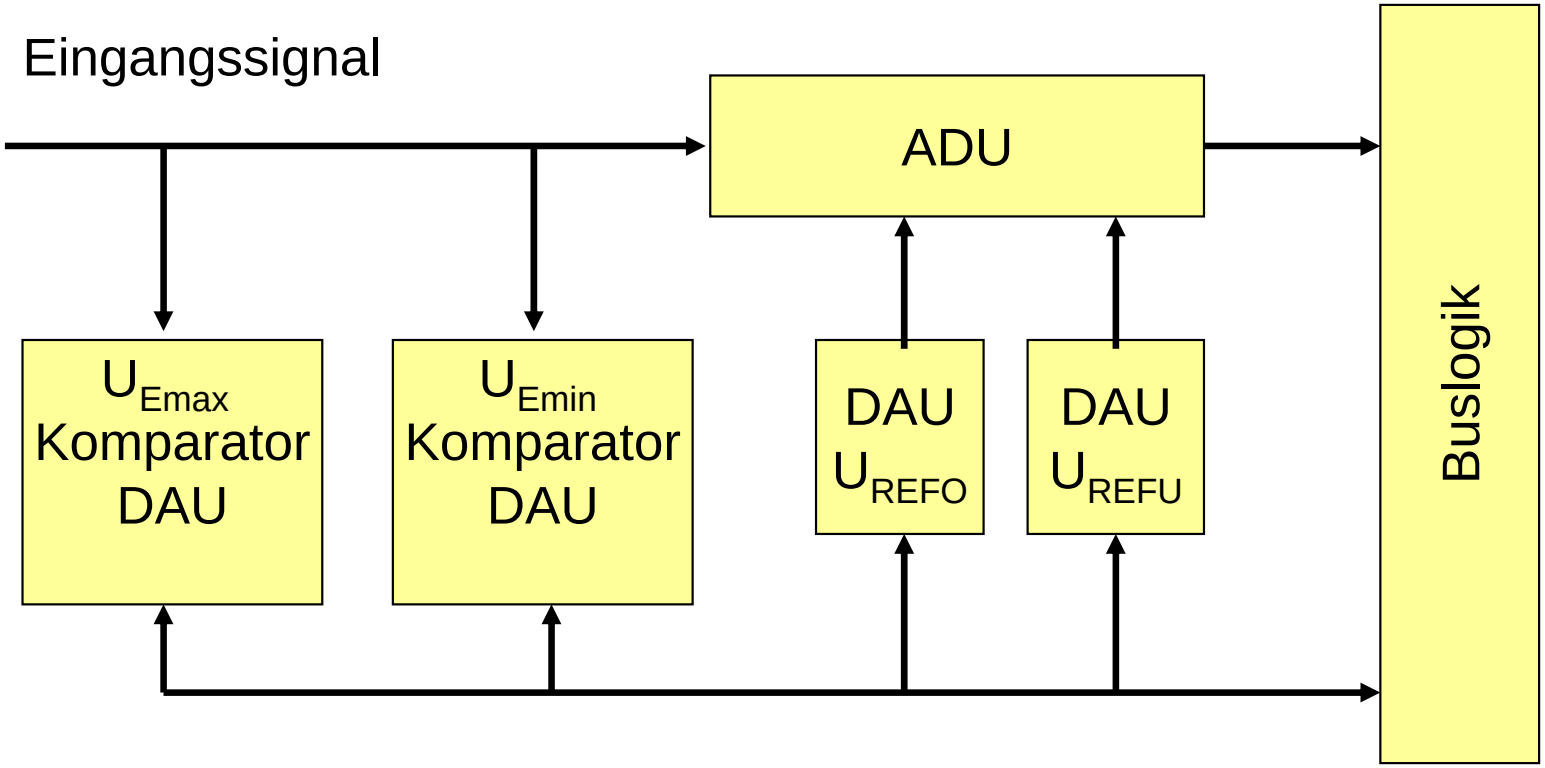



DAU Wandlerfenster



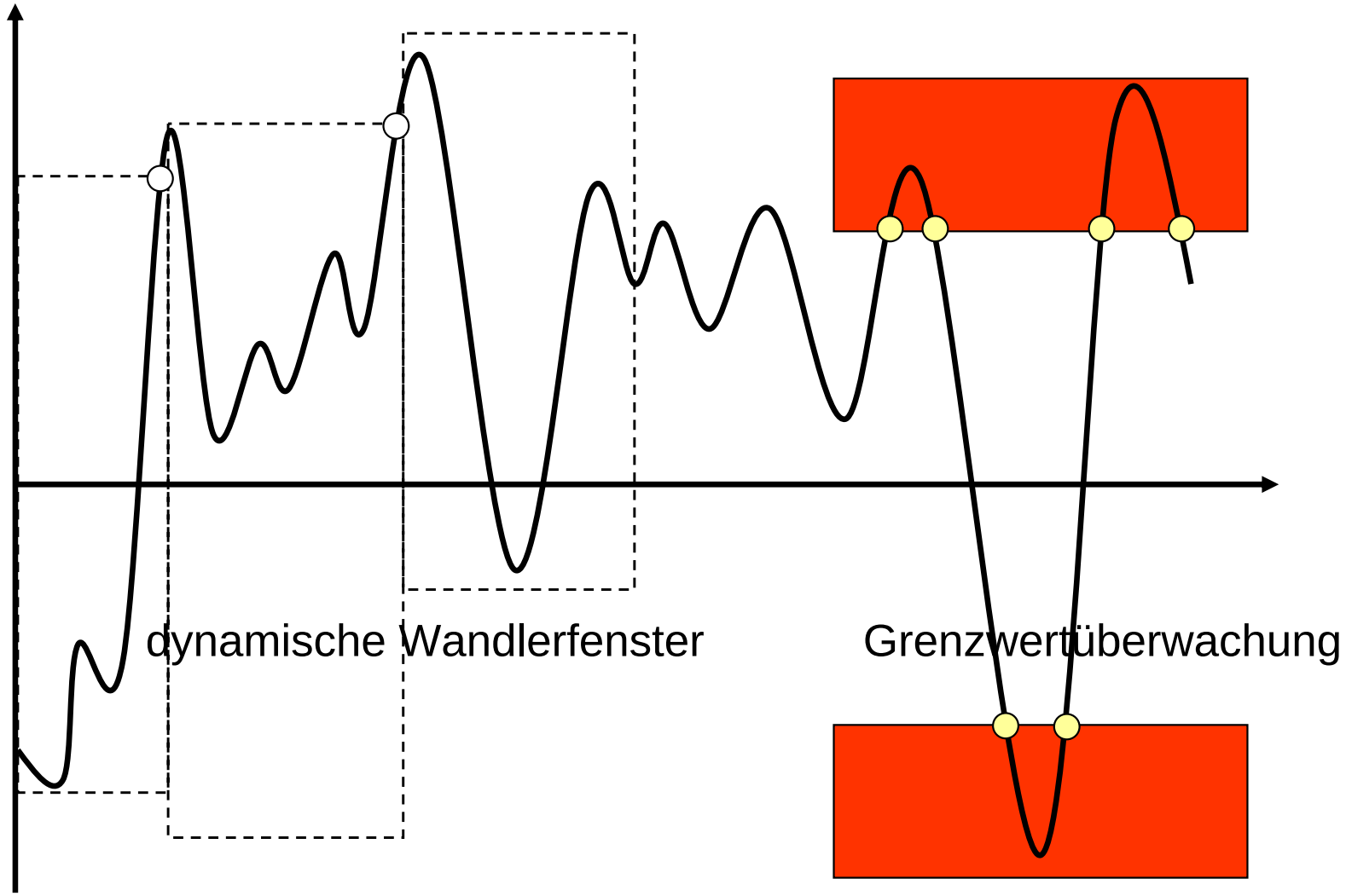

ADU Wandlerfenster

# AD-Umsetzer
## Universeller ADU



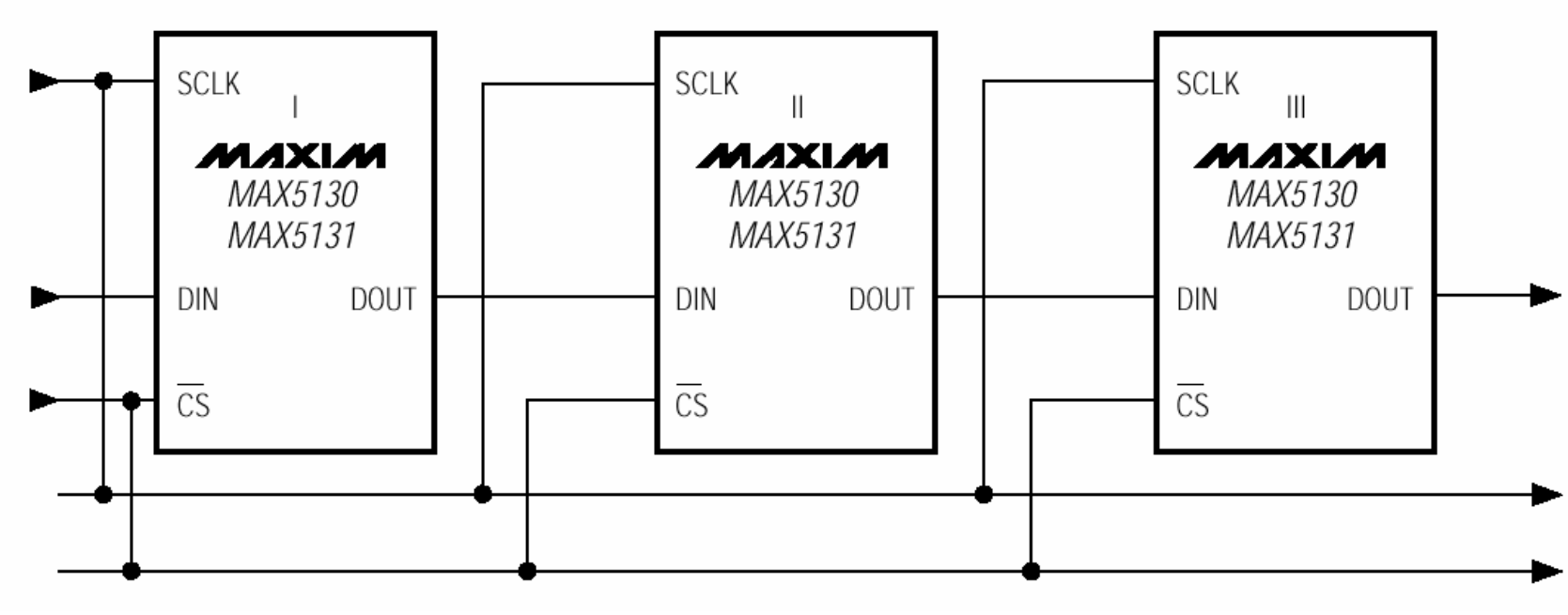
# Analogwerterfassung

mit dynamischen Wandlerfenstern und Grenzwertüberwachung



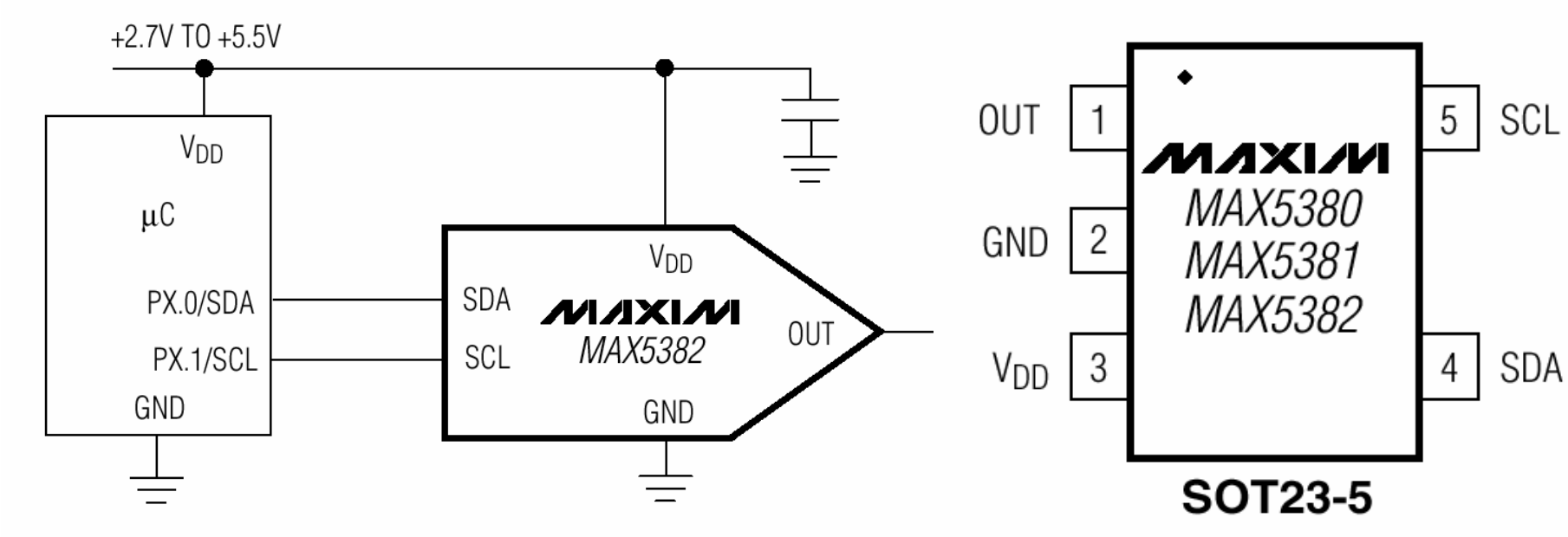
# DAU MAX5130

seriell in Reihe schaltbare DAU



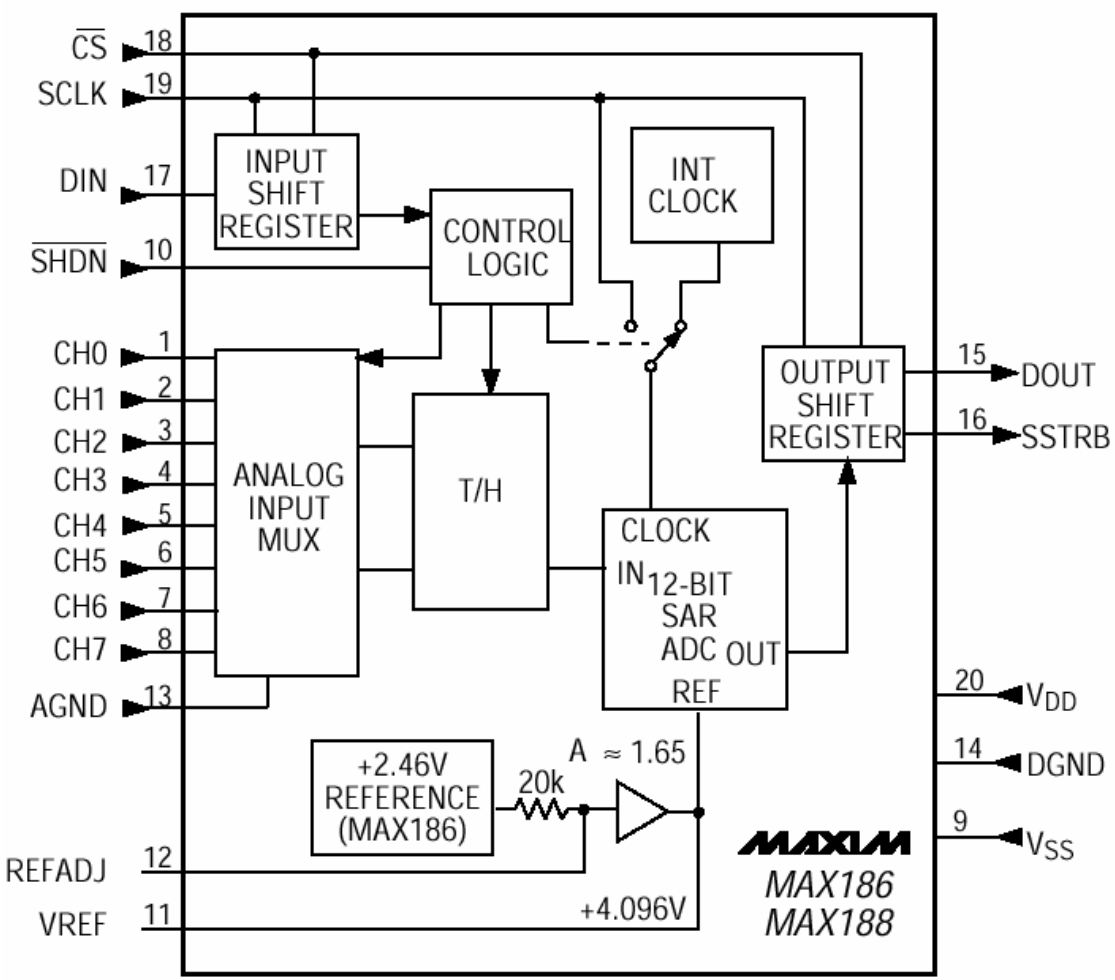
# DAU MAX5382

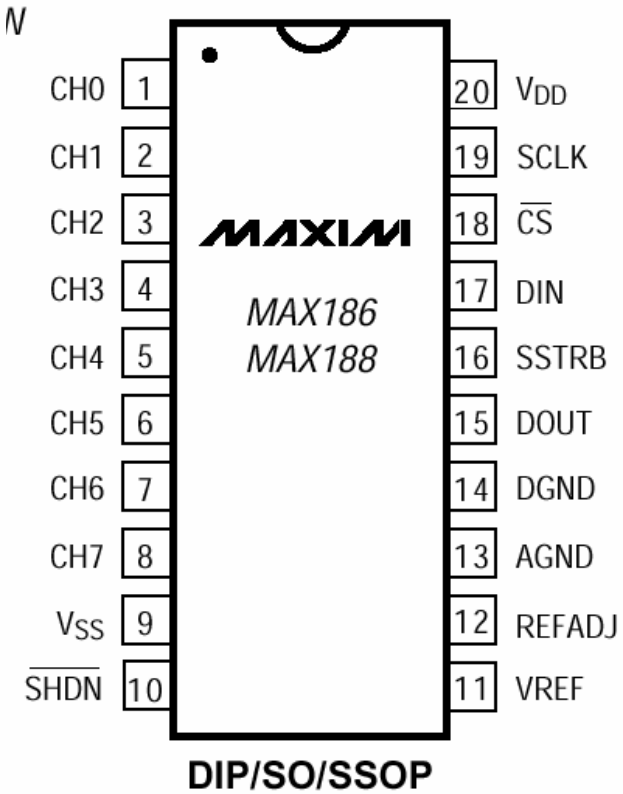
seriell ansteuerbarer DAU mit minimalen Abmessungen

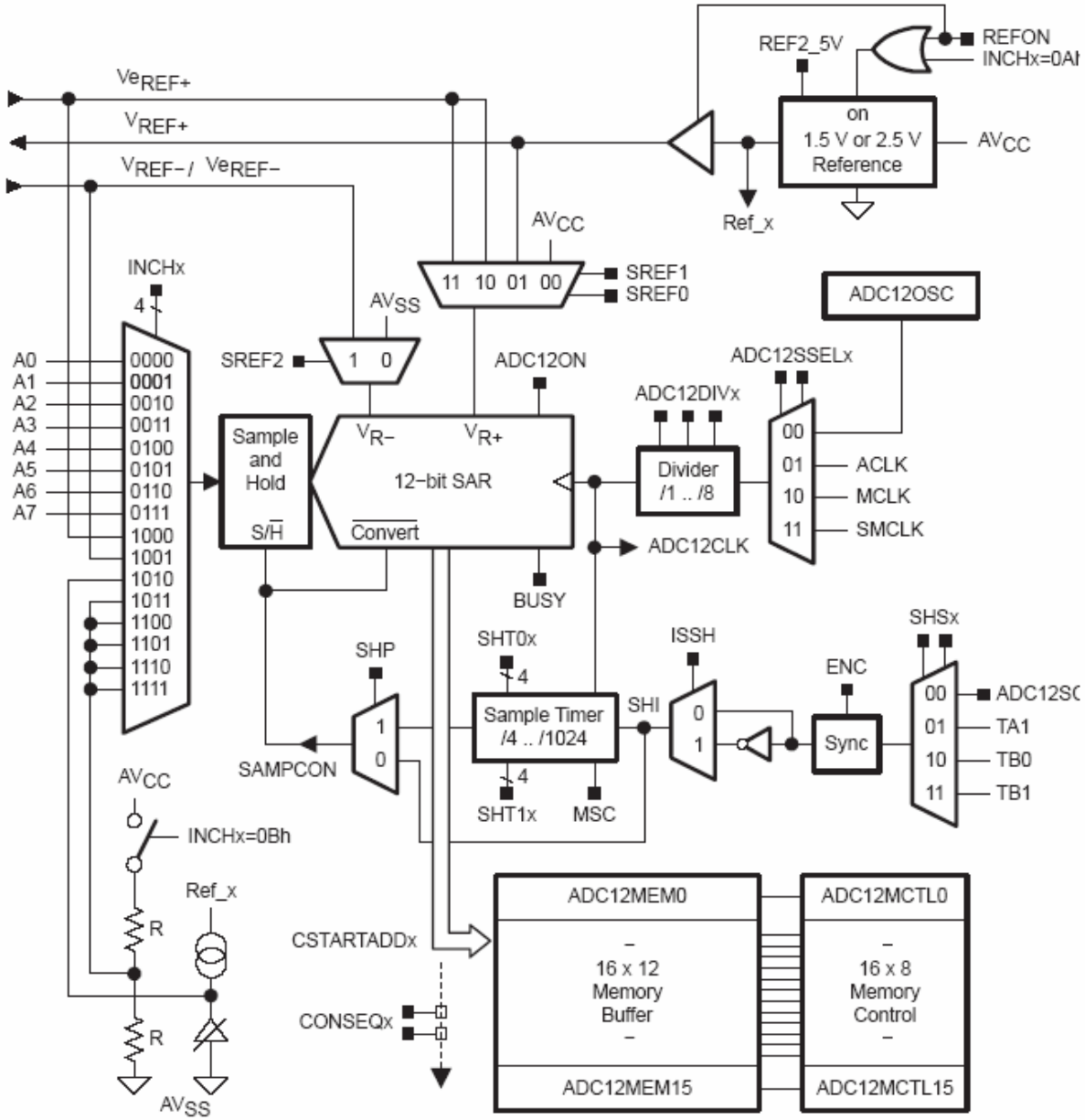


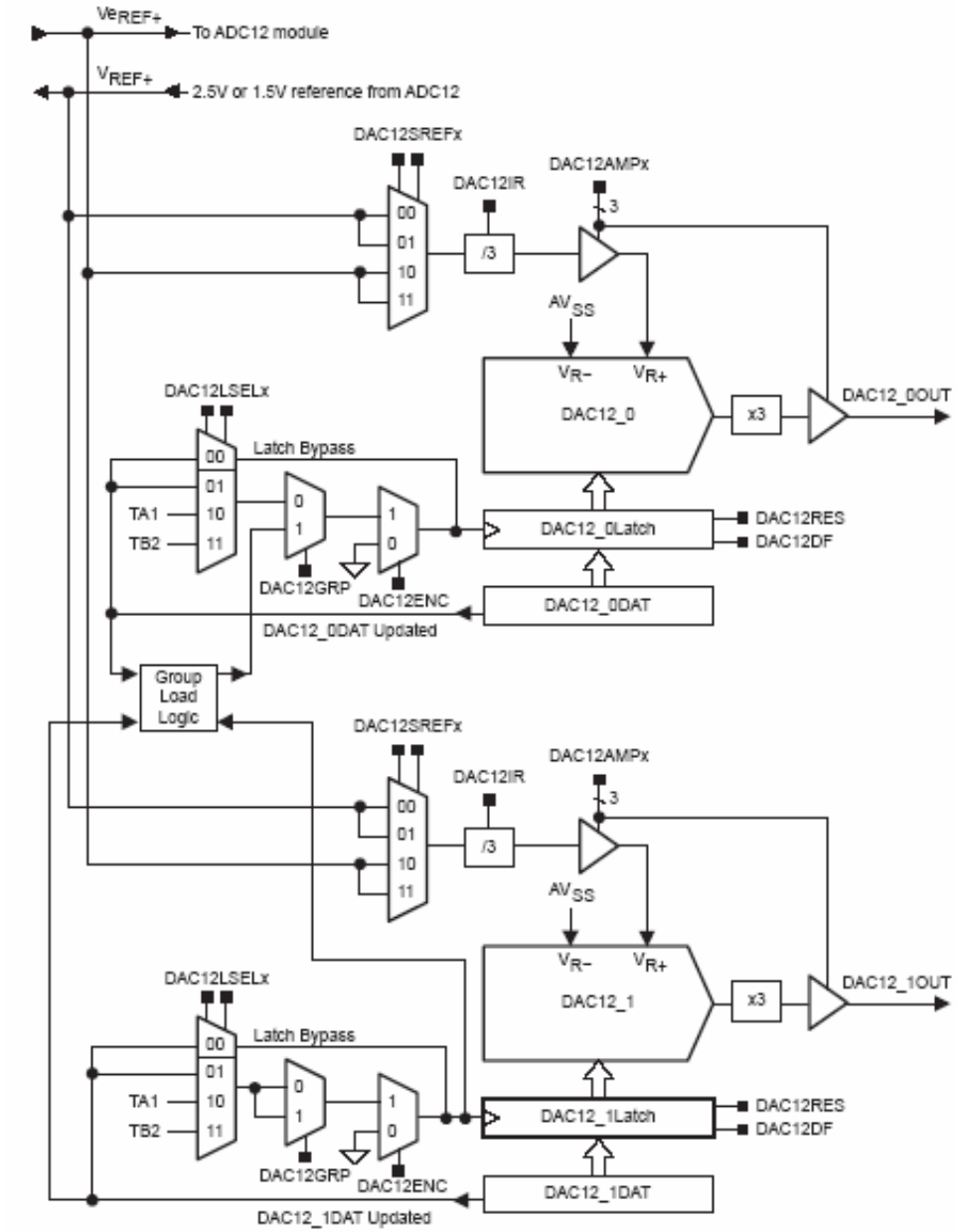
# ADU MAX186

auf Basis der sukzessiven Approximation




REF2_5V
REFON
INCHx=0Ah
on
1.5 V or 2.5 V
Reference
AVCC
Ref_x
VeREF+
VREF+
VREF−/ VeREF−
AVCC
11 10 01 00
SREF1
SREF0
ADC12OSC
INCHx
4
AVSS
SREF2
1 0
ADC12ON
ADC12SSELx
ADC12DIVx
A0
A1
A2
A3
A4
A5
A6
A7
0000
0001
0010
0011
0100
0101
0110
0111
1000
1001
1010
1011
1100
1101
1110
1111
Sample
and
Hold
S/H
VR−
VR+
12−bit SAR
Convert
Divider
/1 .. /8
00
01
10
11
ACLK
MCLK
SMCLK
ADC12CLK
BUSY
SHSx
SHP
SHT0x
ISSH
ENC
ADC12SC
Sample Timer
/4 .. /1024
SHI
Sync
TA1
TB0
TB1
SAMPCON
SHT1x
MSC
AVCC
INCHx=0Bh
Ref_x
R
R
AVSS
CSTARTADDx
CONSEQx
ADC12MEM0
16 x 12
Memory
Buffer
ADC12MEM15
ADC12MCTL0
16 x 8
Memory
Control
ADC12MCTL15


VeREF+
To ADC12 module
VREF+
2.5V or 1.5V reference from ADC12
DAC12SREFx
DAC12IR
DAC12AMPx
00
01
10
11
/3
3
AVSS
VR−
VR+
DAC12_0
x3
DAC12_0OUT
DAC12LSELx
Latch Bypass
TA1
TB2
DAC12_0Latch
DAC12RES
DAC12DF
DAC12GRP
DAC12ENC
DAC12_0DAT
DAC12_0DAT Updated
Group Load Logic
DAC12_1
DAC12_1OUT
DAC12_1Latch
DAC12_1DAT
DAC12_1DAT Updated

# Anwendungsbereites Wissen

- Analoge Signale und Codierungen
- DA-Umsetzerverfahren
- AD-Umsetzerverfahren
- Track&Hold Schaltung
- Sample&Hold Schaltung
- Möglichkeiten dynamischer Wandlungsfenster